



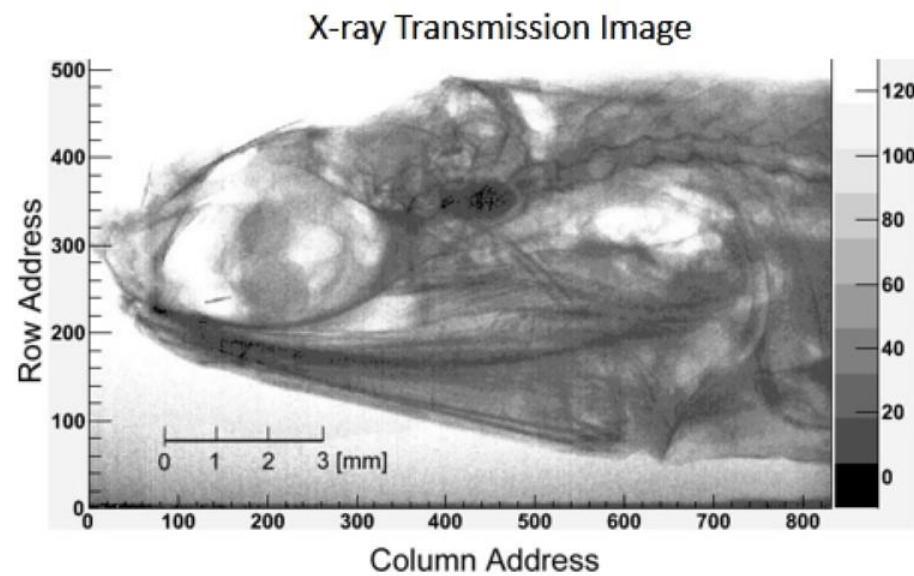
# KEK発測定器技術: SOIピクセルセンサー開発の現状と将来

九州大学セミナー

幅 淳二 KEK、測定器開発室

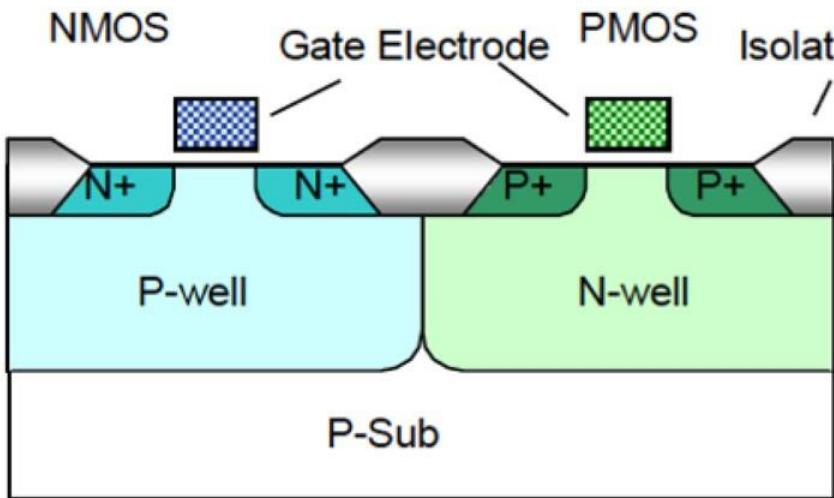
# Outline

- I. はじめに
- II. Process 開発
- III. SOI Pixel検出器紹介
- IV. まとめ

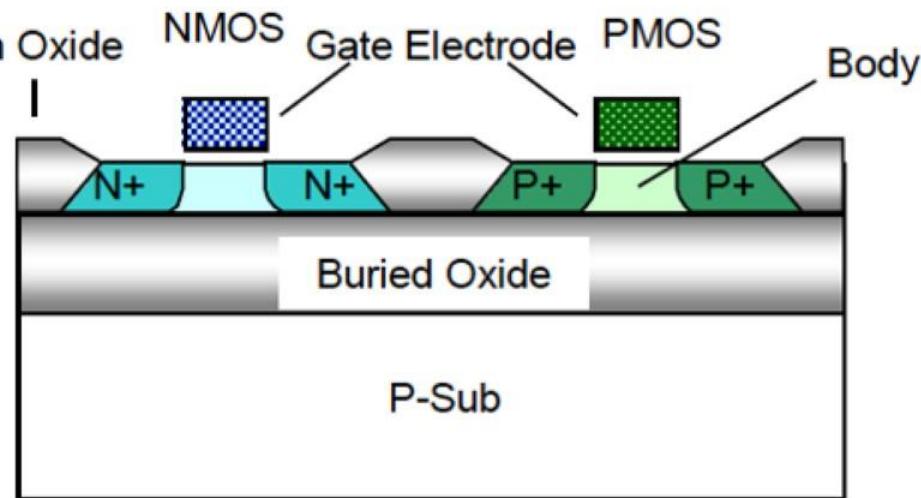


# 1. はじめに

## 通常のLSI



## Silicon-On-Insulator (SOI)



Well構造によるP-N逆バイアスで  
トランジスタを分離

酸化膜でトランジスタを分離。  
寄生容量が少ない。  
高速、低消費電力、高周波向き

# SOI Waferの作り方 I (SIMOX)

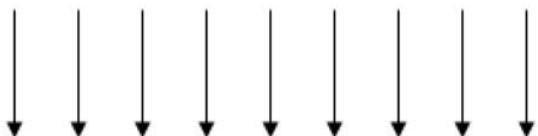


世界で初めてSOIウェハを実用化。

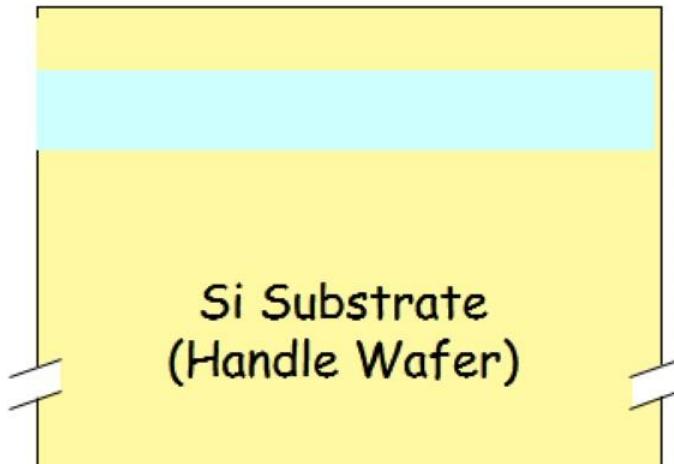
酸素イオンを打ち込み熱処理で酸化膜を生成。

酸素注入・熱処理に時間がかかり、生産性が悪く、高価

Oxygen Ion Implantation  
120-200 keV,  $4-20 \times 10^{17} \text{ cm}^{-2}$



SIMOX  
(Separation by Implanted Oxygen)  
K. Izumi (NTT Japan, 1978)

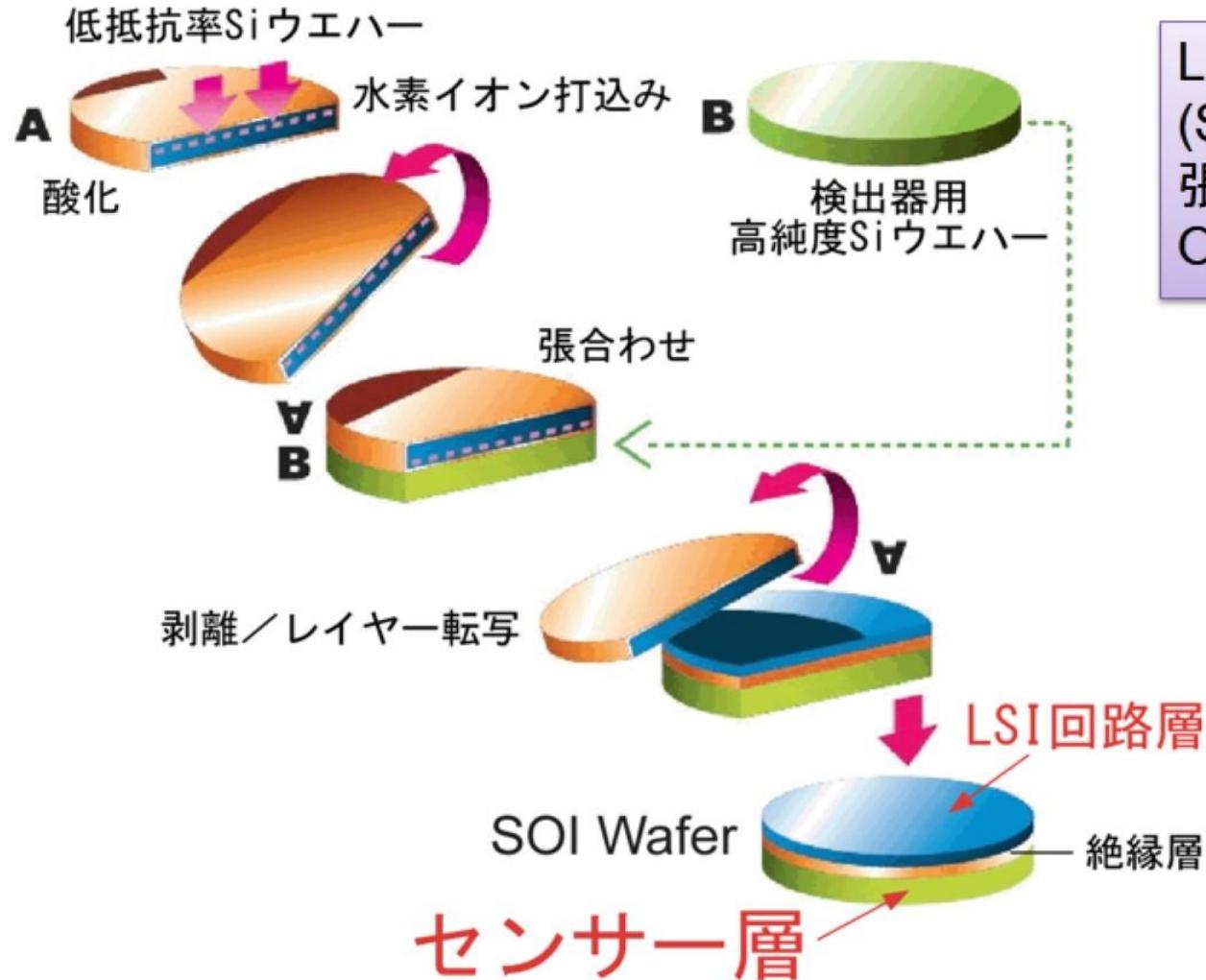


annealing  
3-6 hours  
~1300 °C



# SOI Waferの作り方 II (SmartCut)

現在の主流



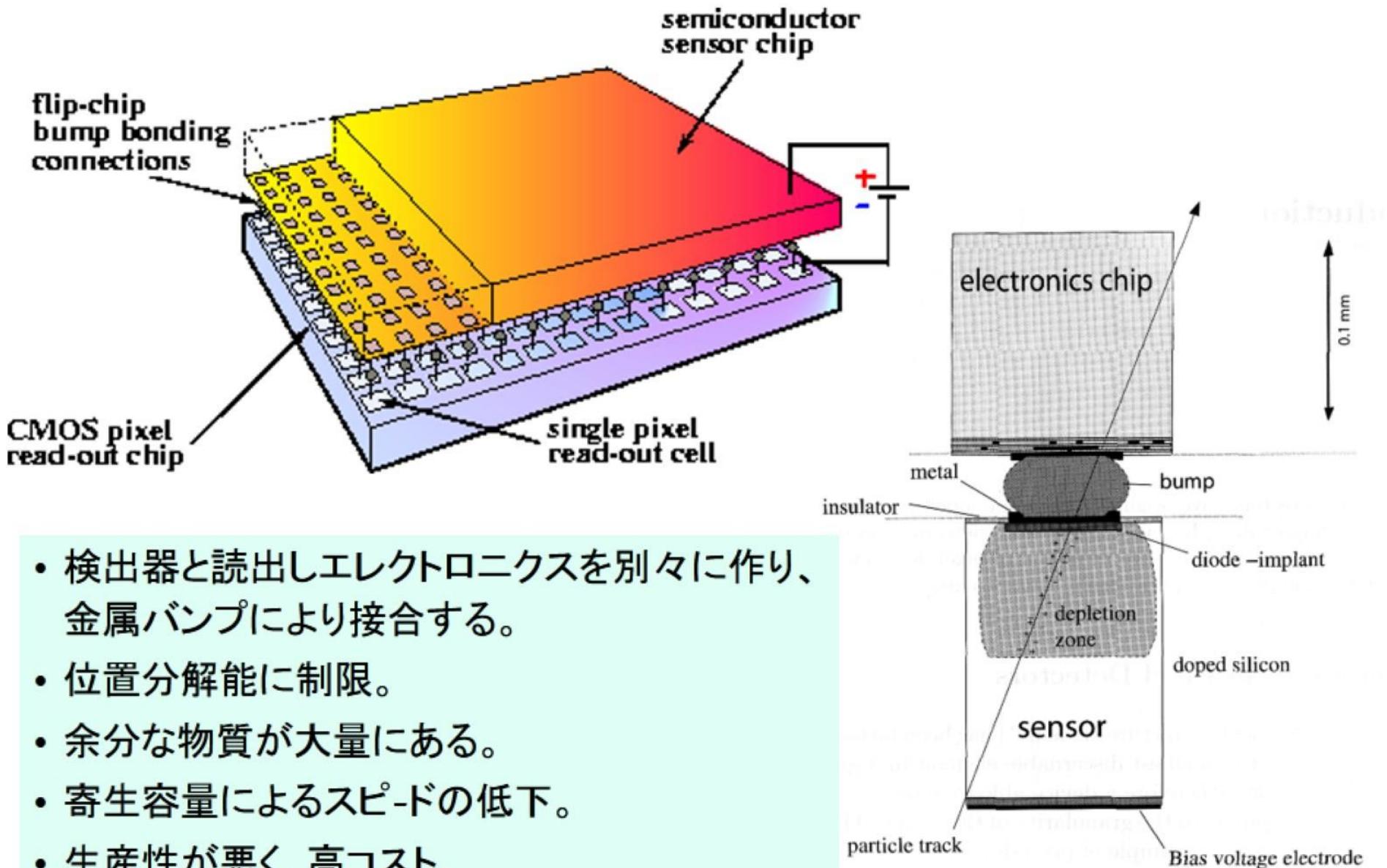
Layer Transfer技術  
(SmartCut)による  
張合わせウエハ Silicon-On-Insulator (SOI)



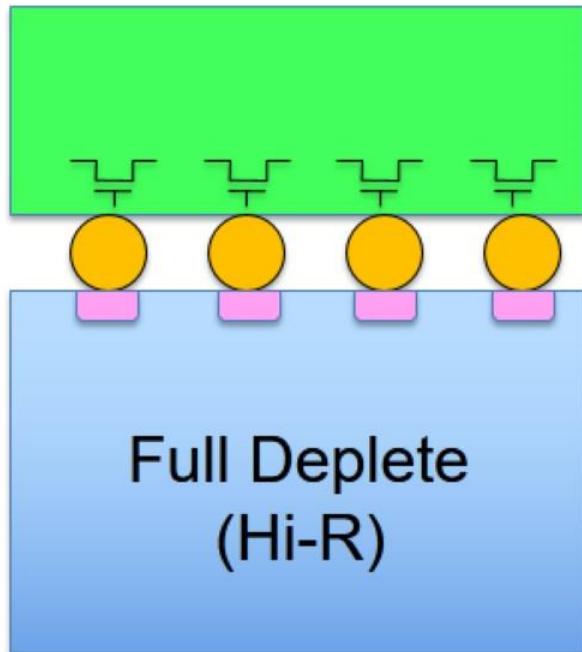
1991 : Michel Bruel of Leti(仏)

2種類のウエハを使うことから、モノリシック検出器への応用が可能。

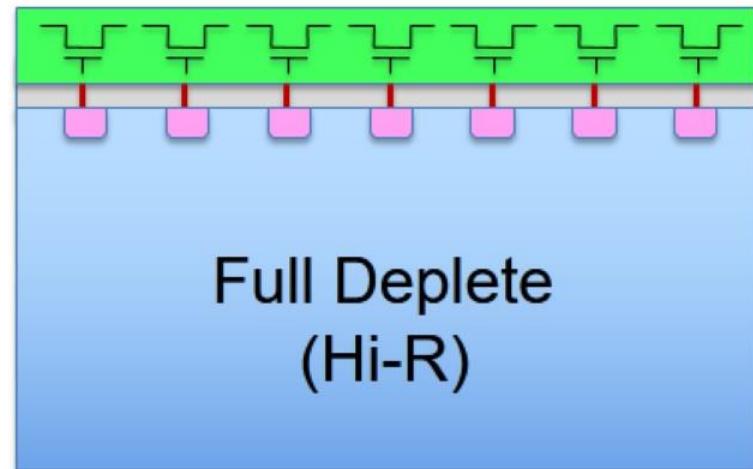
# CERN LHC実験で用いられているPixel検出器(Hybrid Pixel)



## Hybrid Detector



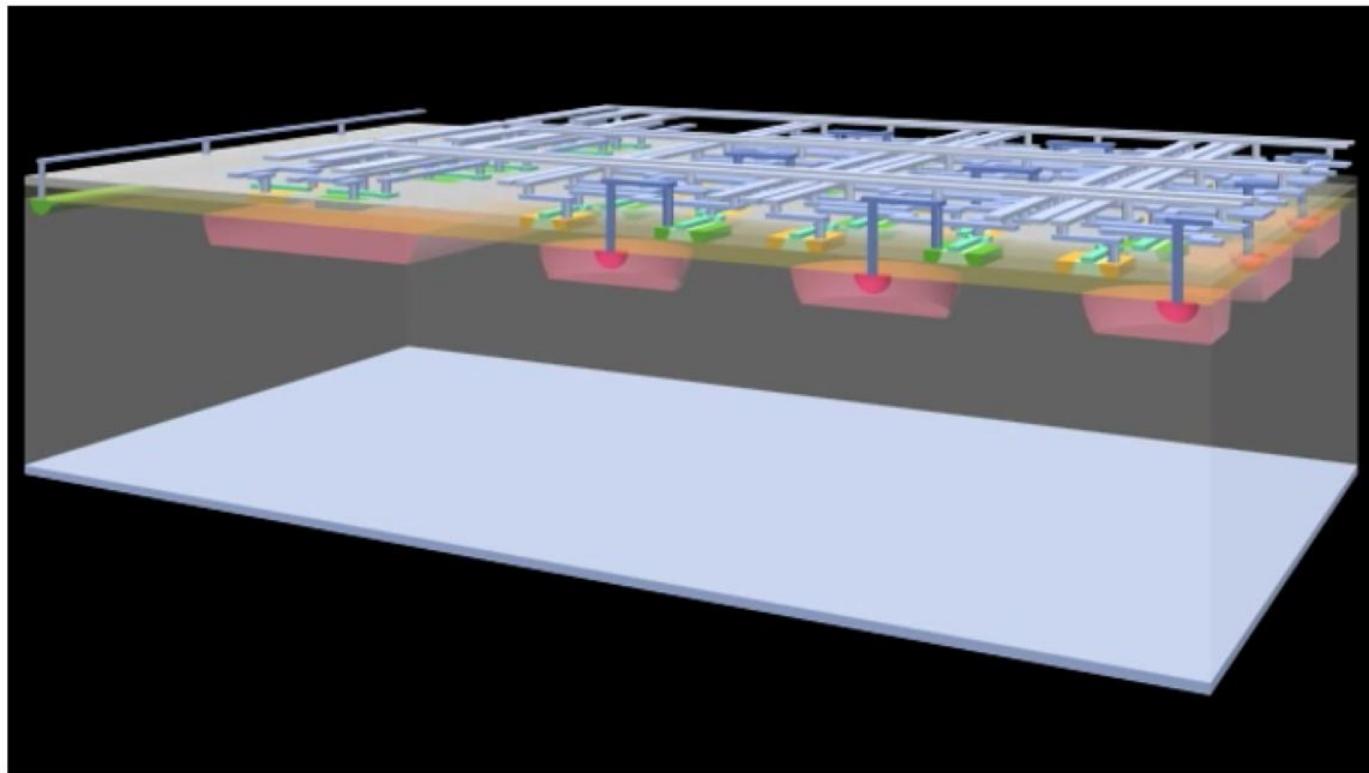
## Silicon-On-Insulator (SOI)



To use SOI technology for pixel detector is already discussed in 1990<sup>(\*)</sup>.

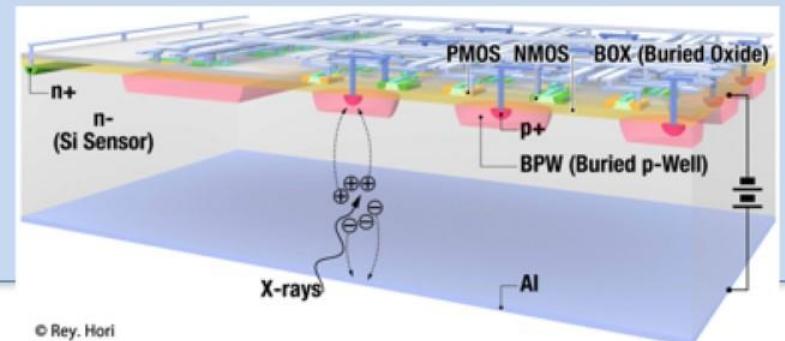
(\*) Jean-Pierre Colinge, 'An overview of CMOS-SOI technology and its potential use in particle detection systems', NIM A305 (1991) 615-619.

## II. SOI Pixel Process 開発



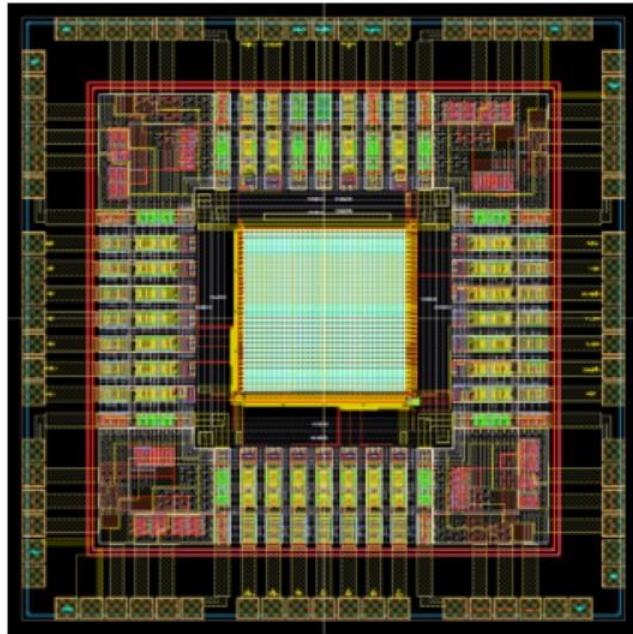
# SOI Pixel検出器の特徴

- 機械的接合がなく、半導体微細加工のみで製造。  
高信頼性、高分解能、低価格が望める。
- 超薄型センサ( $\sim 50\mu\text{m}$ )による、多重散乱を防ぐ荷電粒子検出。  
厚い空乏層( $\sim 500\mu\text{m}$ )による、X線・赤外線への高い感度。
- ラッチアップがなく、放射線による単発現象にも強い。
- 高度信号処理回路やメモリーを持つインテリジェント・ピクセルが可能に。
- 過酷な環境(極低温、放射線)への強い耐性。
- 基本は産業界の標準技術。  
(技術発展の取り込みが容易)  
日本発の最先端技術。

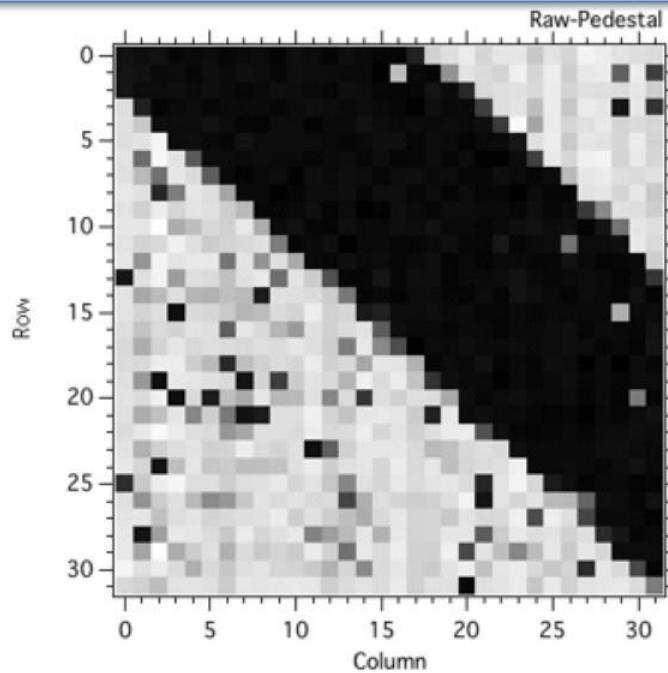


## 2005年測定器開発室スタート

- ・当時日本で独自の半導体Pixel検出器の開発がなかったことから、SOI Pixel検出器開発を開発室プロジェクトとして提案。
- ・NTTからの技術移転で、世界で初めてSOI半導体の実用化を行っていた沖電気(後にラピス・セミコンダクタ)に共同研究を持ちかける。
- ・2005年末に試験チップを投入、2006年に初めてのイメージを取得。

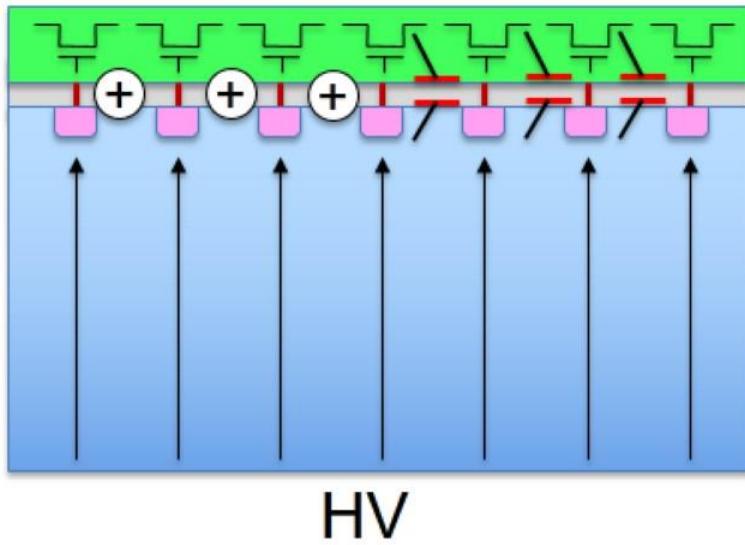


最初の試験チップ



初めてのイメージ  
(チップの前にワイヤーを置いて撮影)

## Issues in SOI Pixel



- Transistors does not work with Detector High Voltage.  
**(Back-Gate Effect)**
- Circuit signal and sense node couples.  
**(Signal Cross Talk)**
- Oxide trapped hole induced by radiation will shift transistor threshold voltage.  
**(Radiation Tolerance)**

1990年代に、いくつかのSOI検出器R&Dがスタート。  
しかし、プロセス技術が未熟で、上記課題を解決できなかった。  
また、良い貼り合わせウエハがなかった。  
→ほとんどのR&Dは失敗のうちに終了。

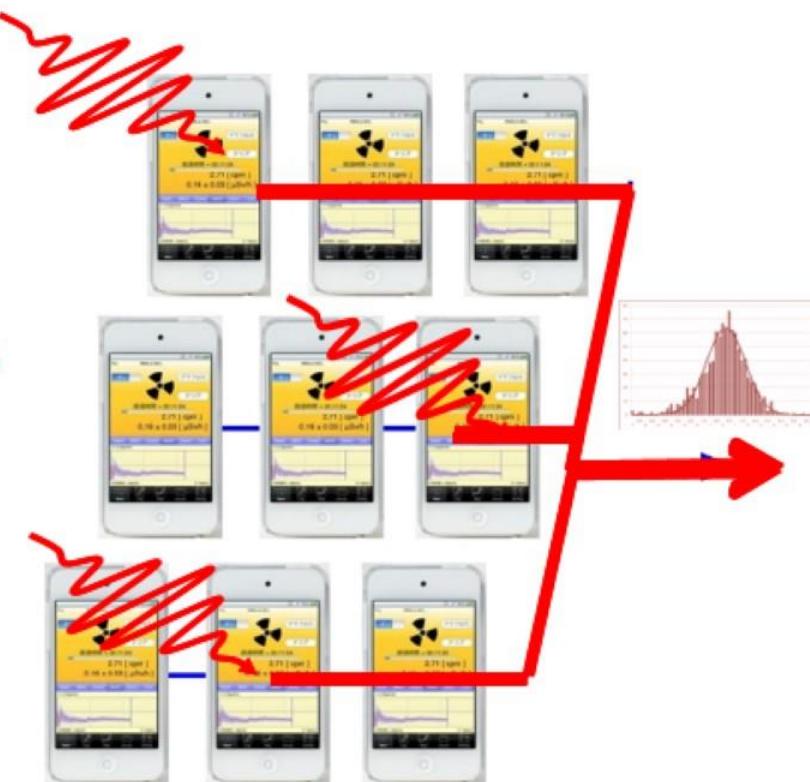
# Revolution of Measurement

Conventional Radiation Detector



Measure Total Charge  
generated by radiation

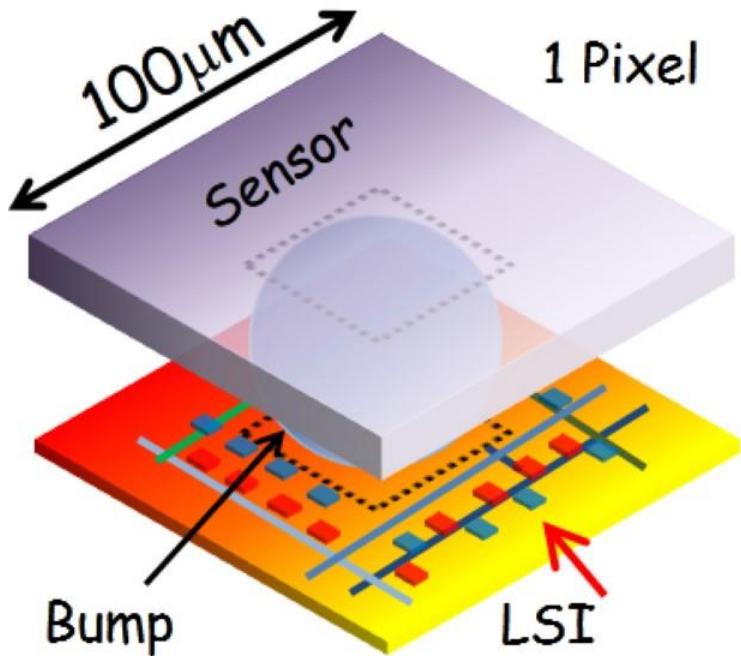
SOIPIX



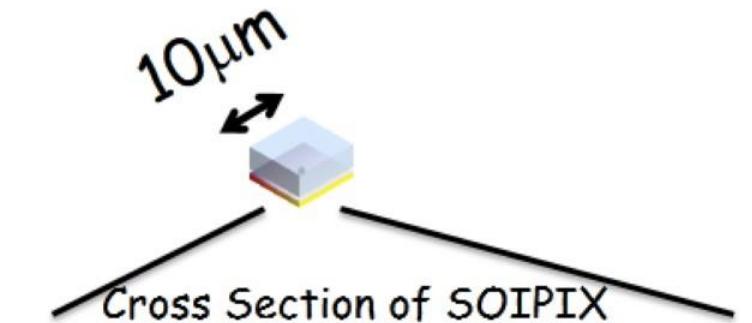
Detect a Quantum  
in each Pixel

# Revolution of Scale

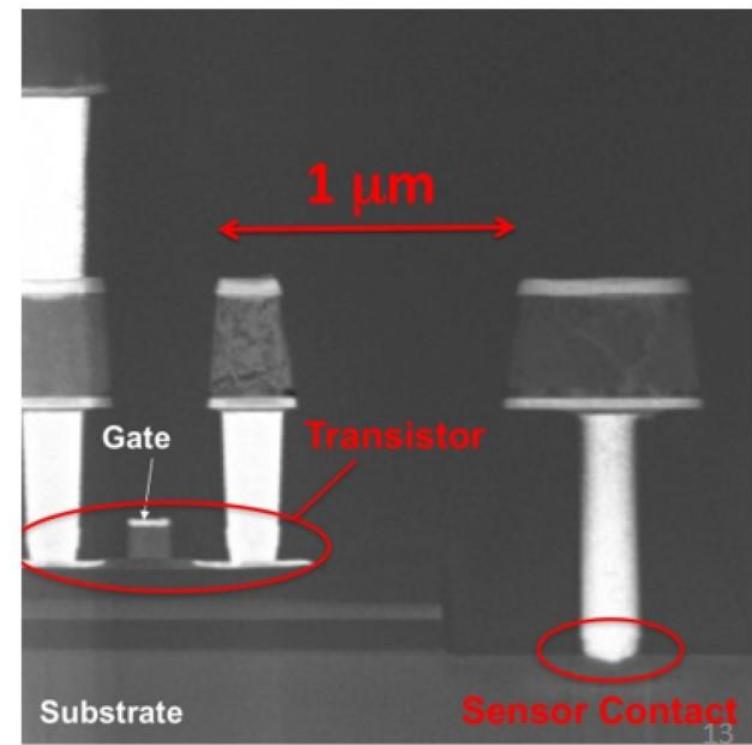
## Hybrid Detector



## SOIPIX



1/100 of Pixel Area!

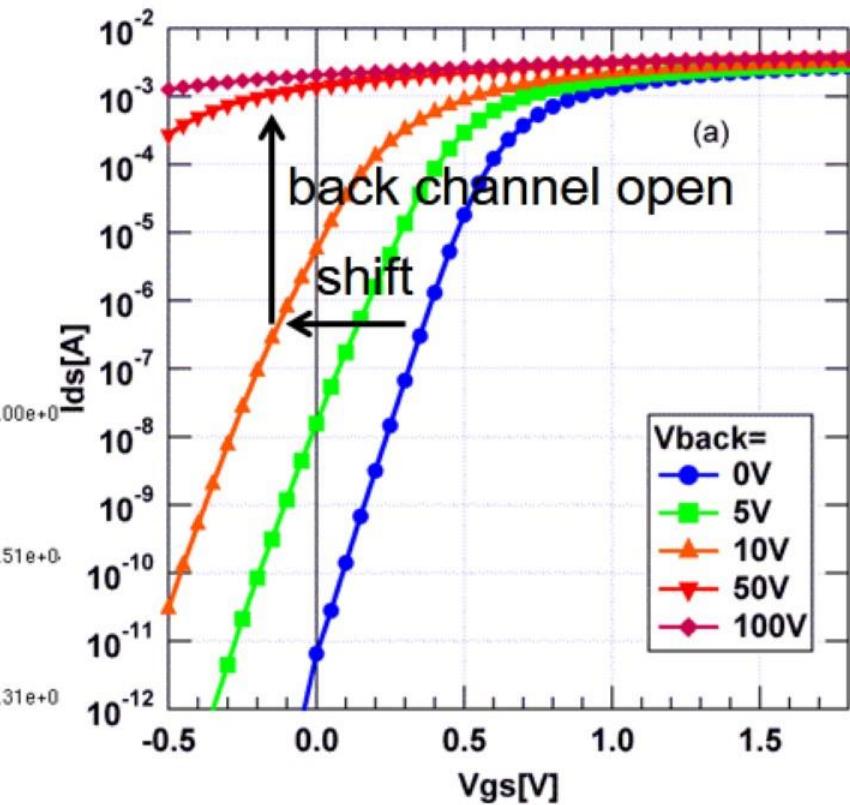
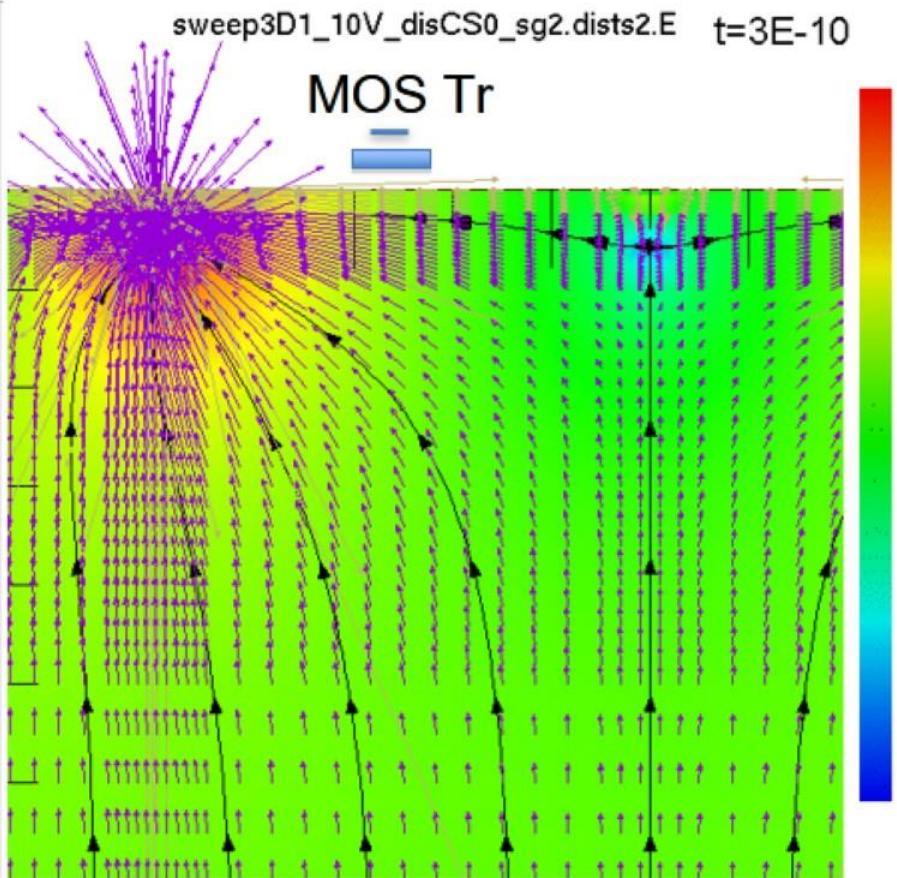


## Lapis Semi.(\*) 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um <sup>2</sup> ), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmφ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) > 2k Ω-cm, FZ(p) ~25 k Ω-cm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

(\*) Former OKI Semiconductor Co. Ltd.

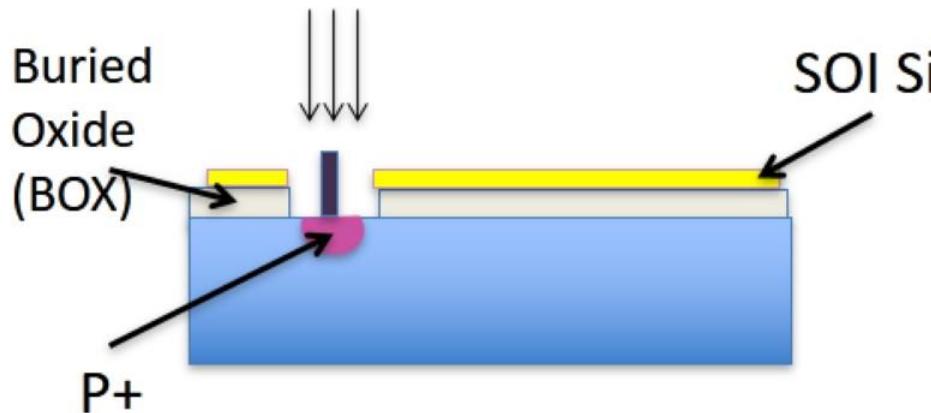
# Main Issue in the SOIPIX: Back-Gate Effect



Detector Voltage act  
as a Back Gate of the  
Transistors, and open  
back channel.

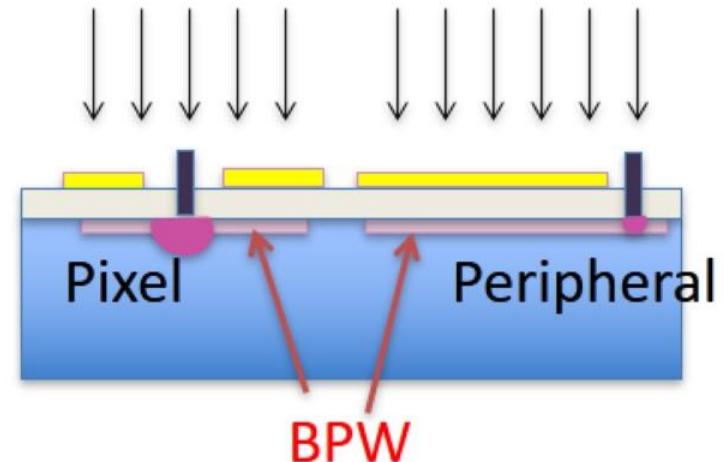
# Buried p-Well (BPW)

## Substrate Implantation



- Cut Top Si and BOX
- High Dose

## BPW Implantation



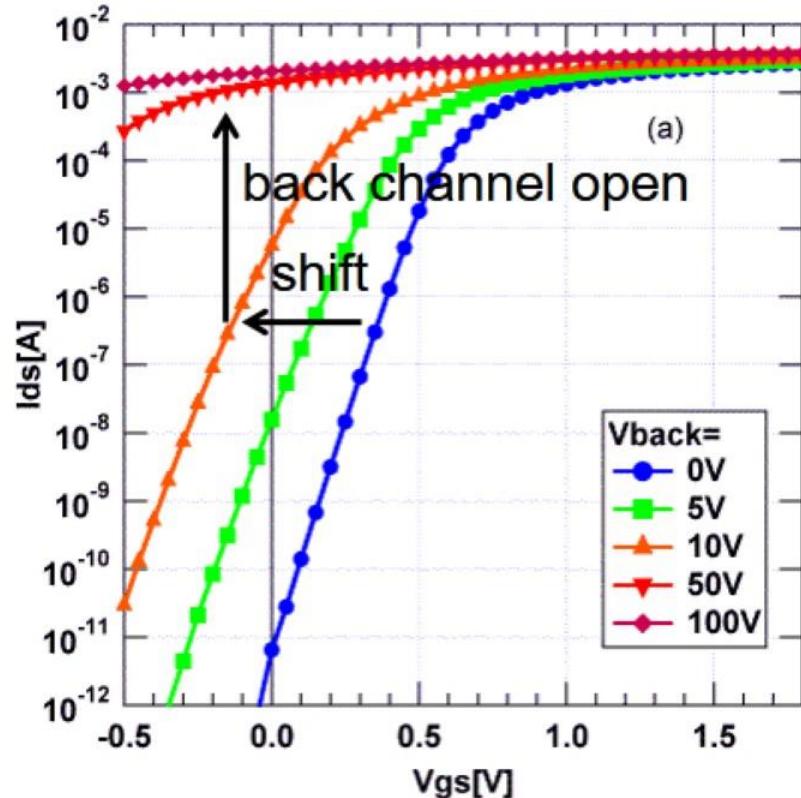
- Keep Top Si not affected
- Low Dose

- Suppress the **Back Gate Effect**.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- Reduce electric field in the BOX which improve radiation hardness.

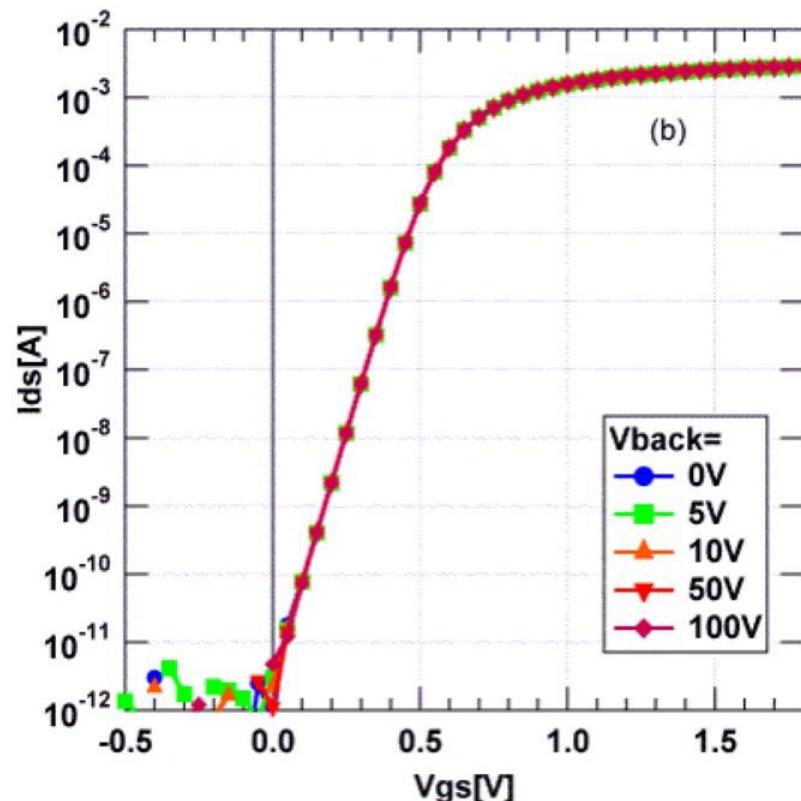
## $I_{ds}$ - $V_{gs}$ and BPW

NMOS

w/o BPW



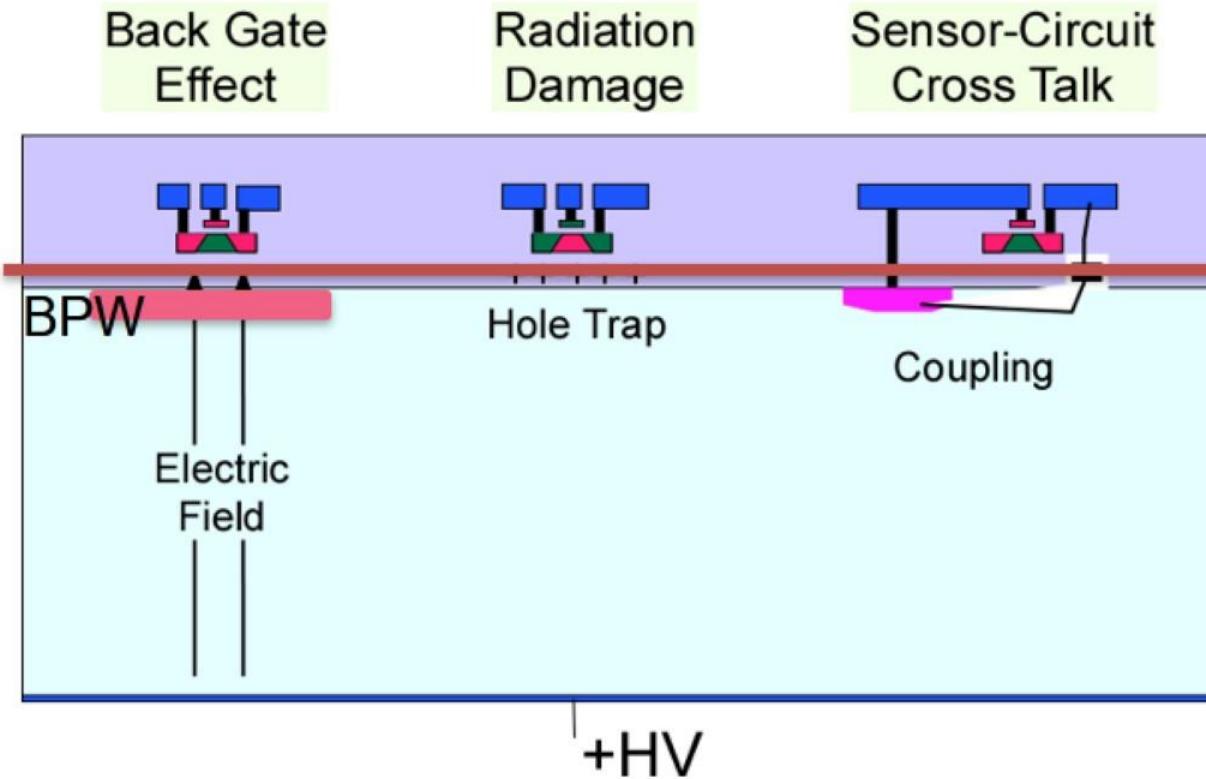
with BPW=0V



Back-gate effect is completely suppressed by the BPW.

# Issues in SOI detector

Sensor and Electronics are located very near. This cause ..

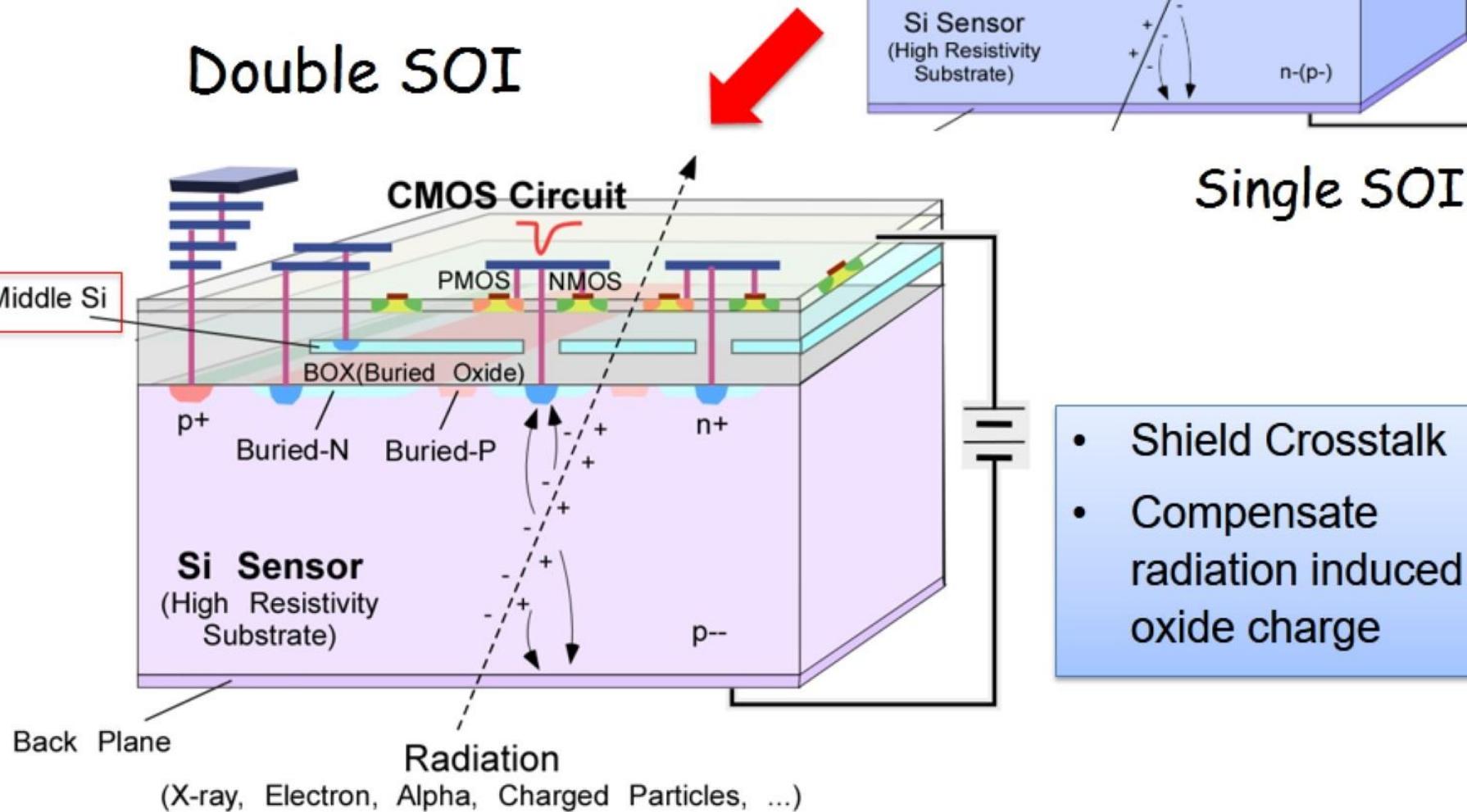


At first, we successfully introduced BPW layer to remove the back gate effect.

Then we newly introduced additional conductive layer under the transistors to reduce all effects ( $\rightarrow$  Double SOI).

## From Single SOI to Double SOI

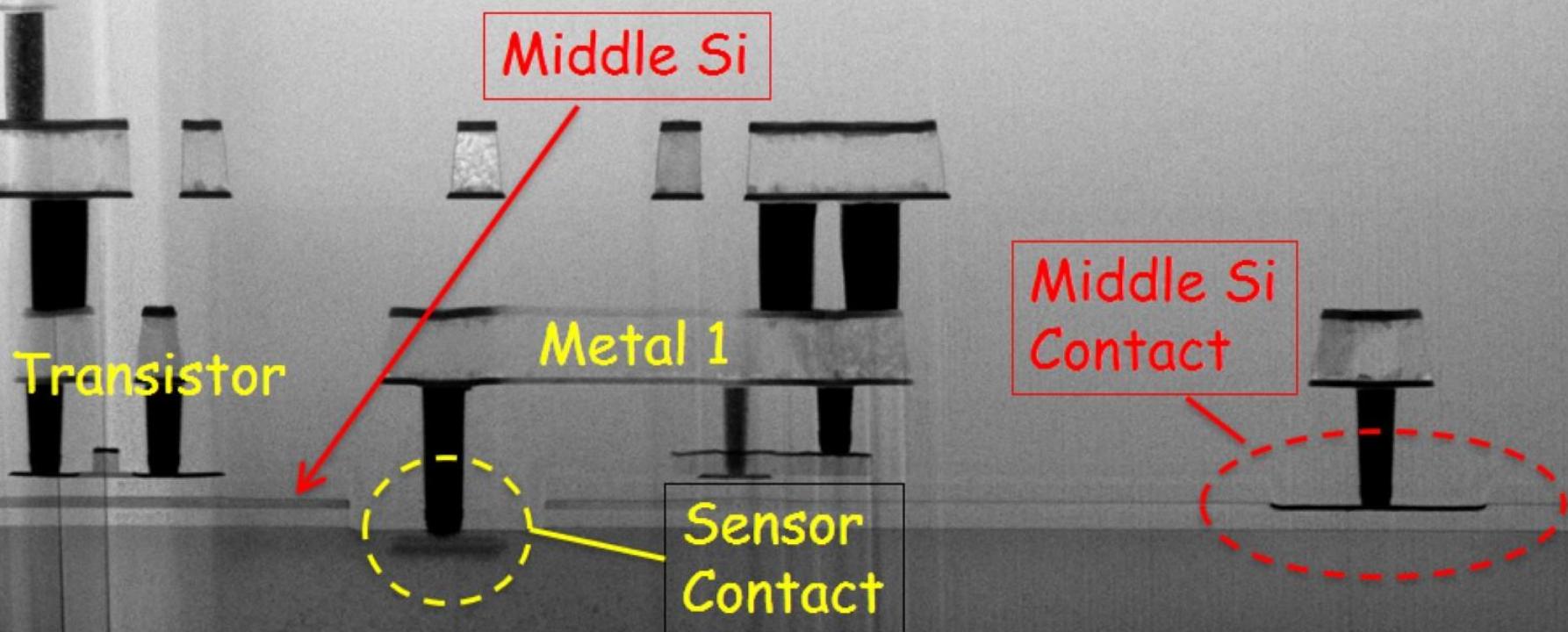
Double SOI



- Shield Crosstalk
- Compensate radiation induced oxide charge

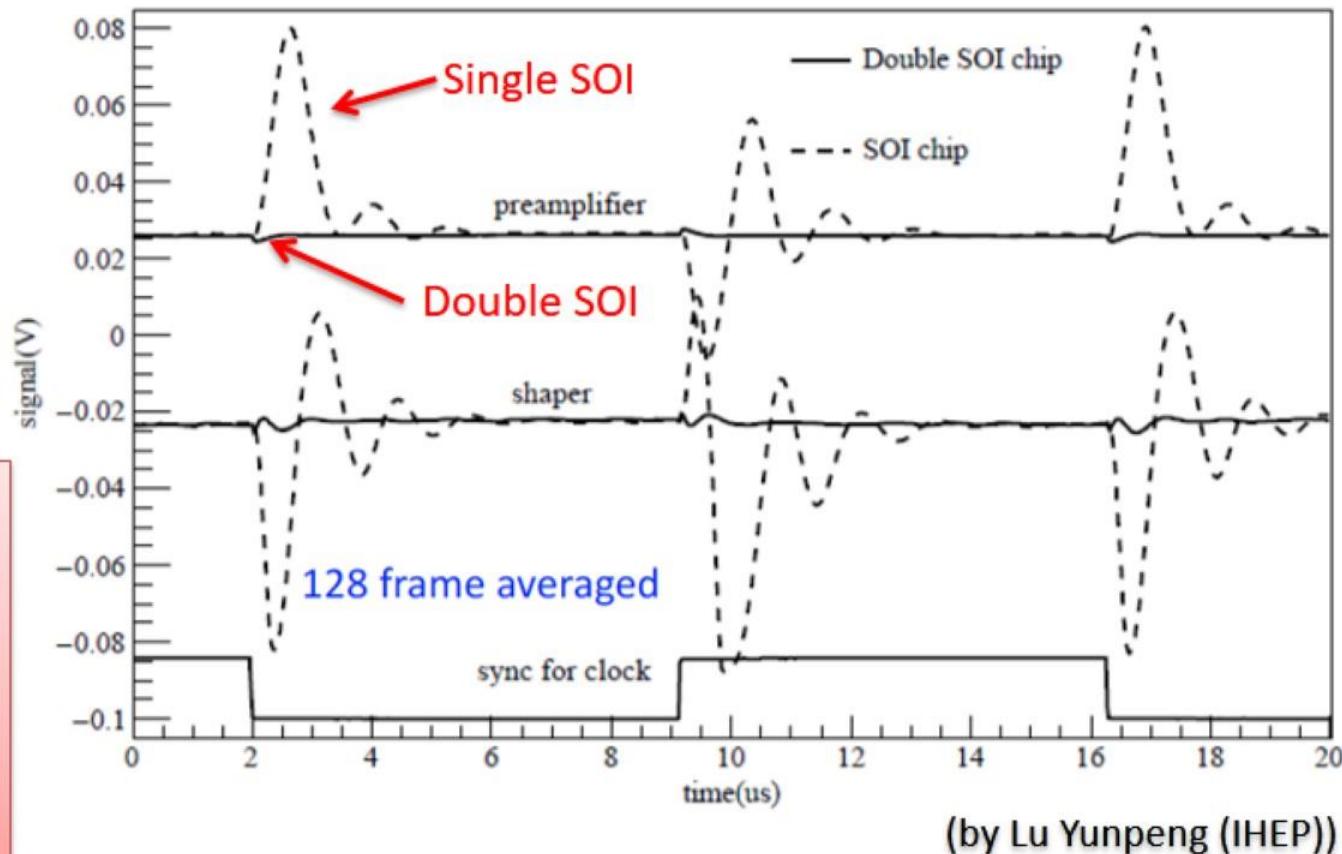
Metal 5

## Cross section of the Double SOI Pixel



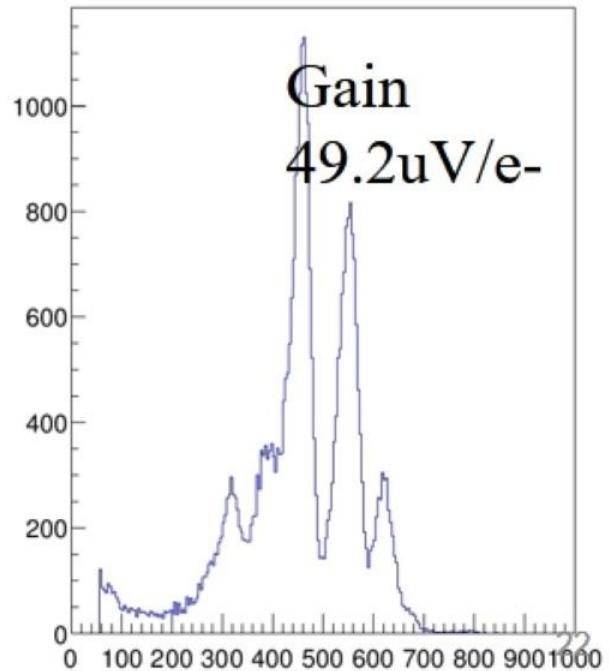
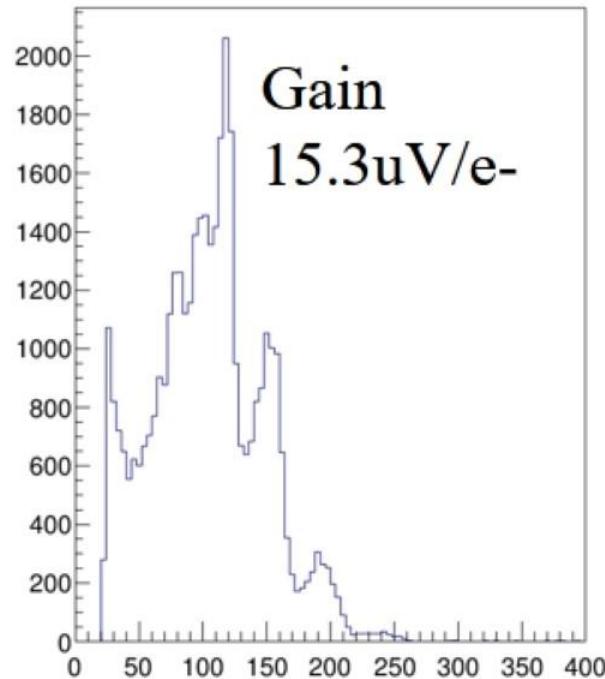
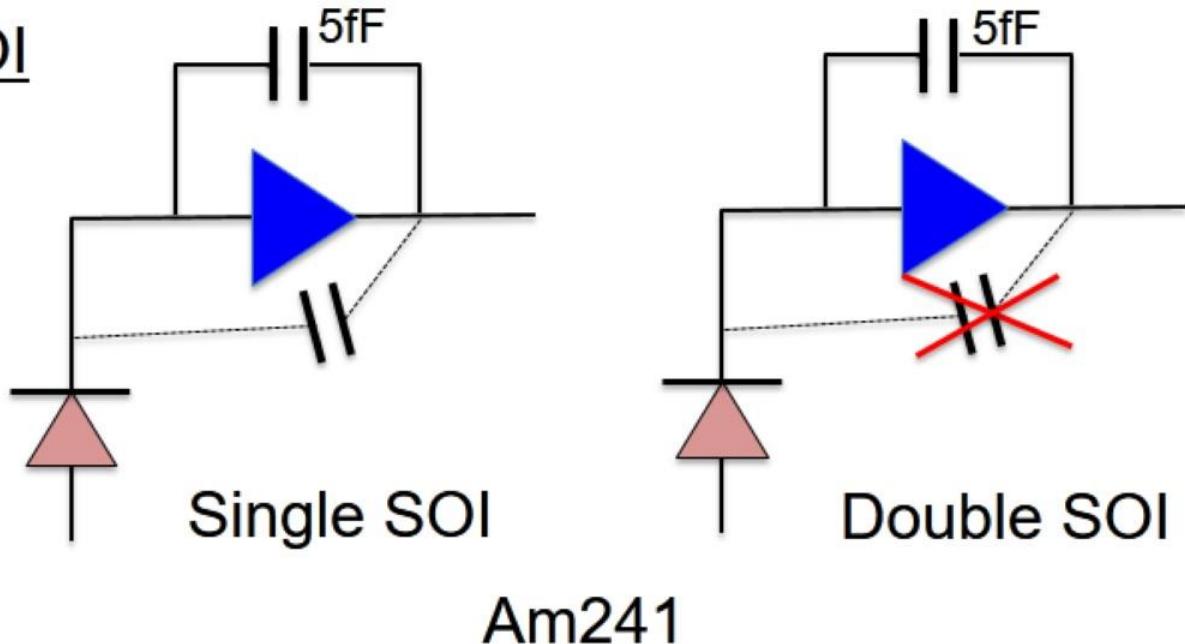
# Effect of Double SOI

## Cross Talk from Clock line



## Effect of Double SOI

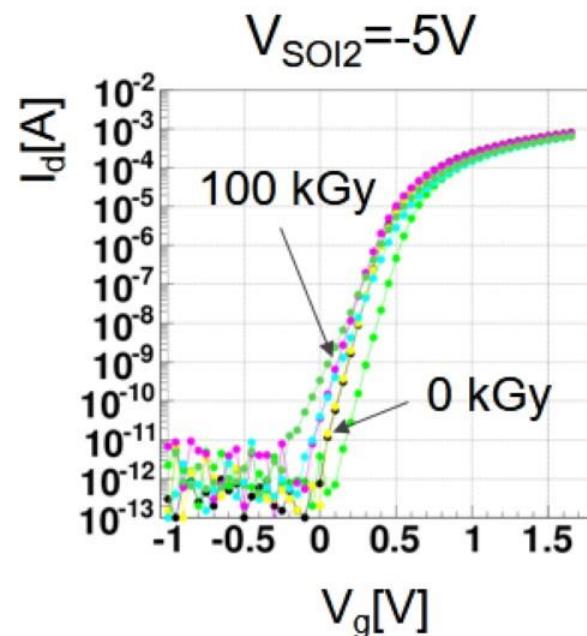
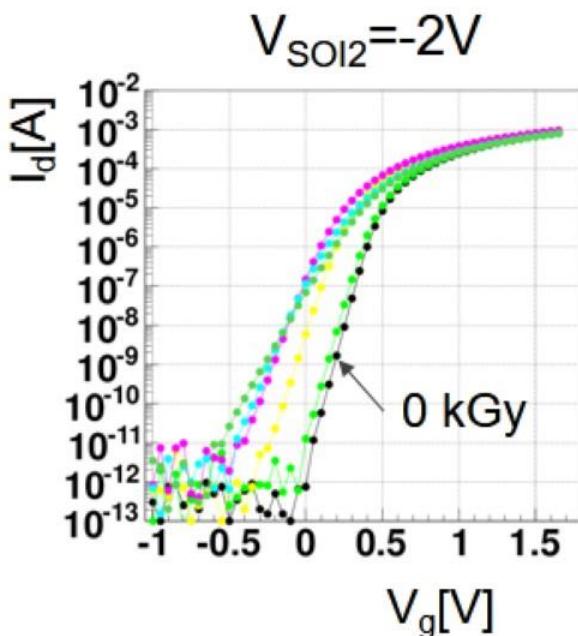
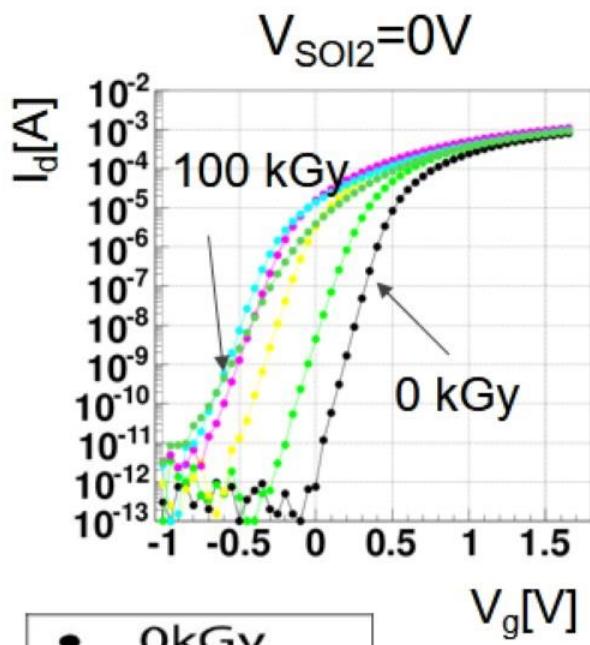
Coupling:  
Gain of Charge  
Amp increases ~3  
times by cutting  
parasitic C.



# Gamma-ray Irradiation Test (Id-Vg Characteristics v.s. SOI2 Potential)

NMOS

I/O normal Vth  
Source-Tie Tr.  
L/W = 0.35um/5um



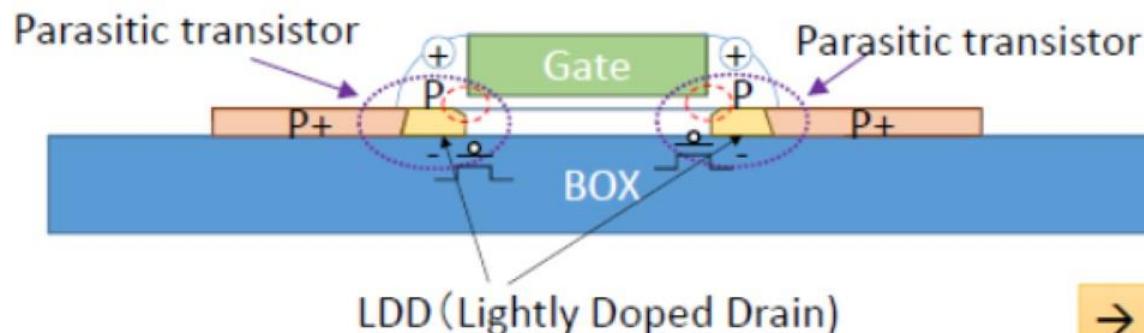
- 0kGy
- 0.5kGy
- 1kGy
- 2kGy
- 5kGy
- 10kGy
- 20kGy
- 100kGy

By setting Middle Si potential ( $V_{soi2}$ ) to -5V, Id-Vg curve returned nearly to pre-irradiation value at 100 kGy(Si) (10 Mrad).

(by U. of Tsukuba)

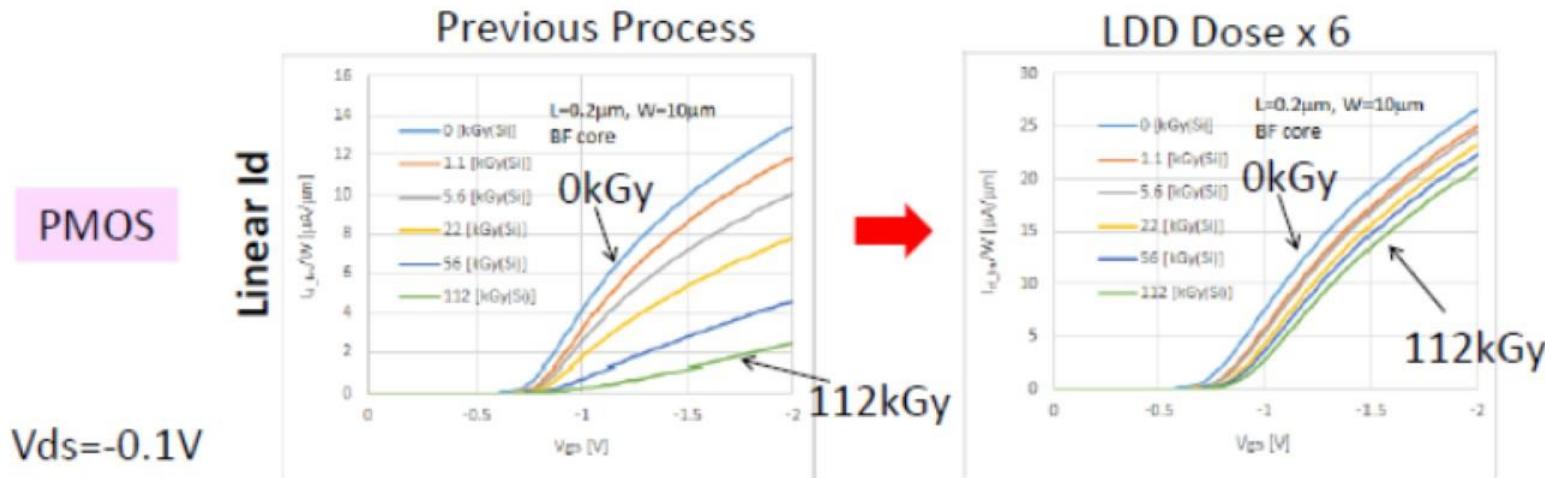
## Dose Increase in Lightly Doped Drain (LDD) Region

- Major cause of the drain current degradation in PMOS with radiation is  $V_{th}$  increase at gate edge due to positive charge generation in spacer.
- Charge in spacer control the  $V_{th}$  of the parasitic transistor.
- To reduce this effect, lightly doped drain (LDD) dose should be increased.
- Present process has rather low dose in LDD region to aiming lower power.



→ Kurachi's Talk

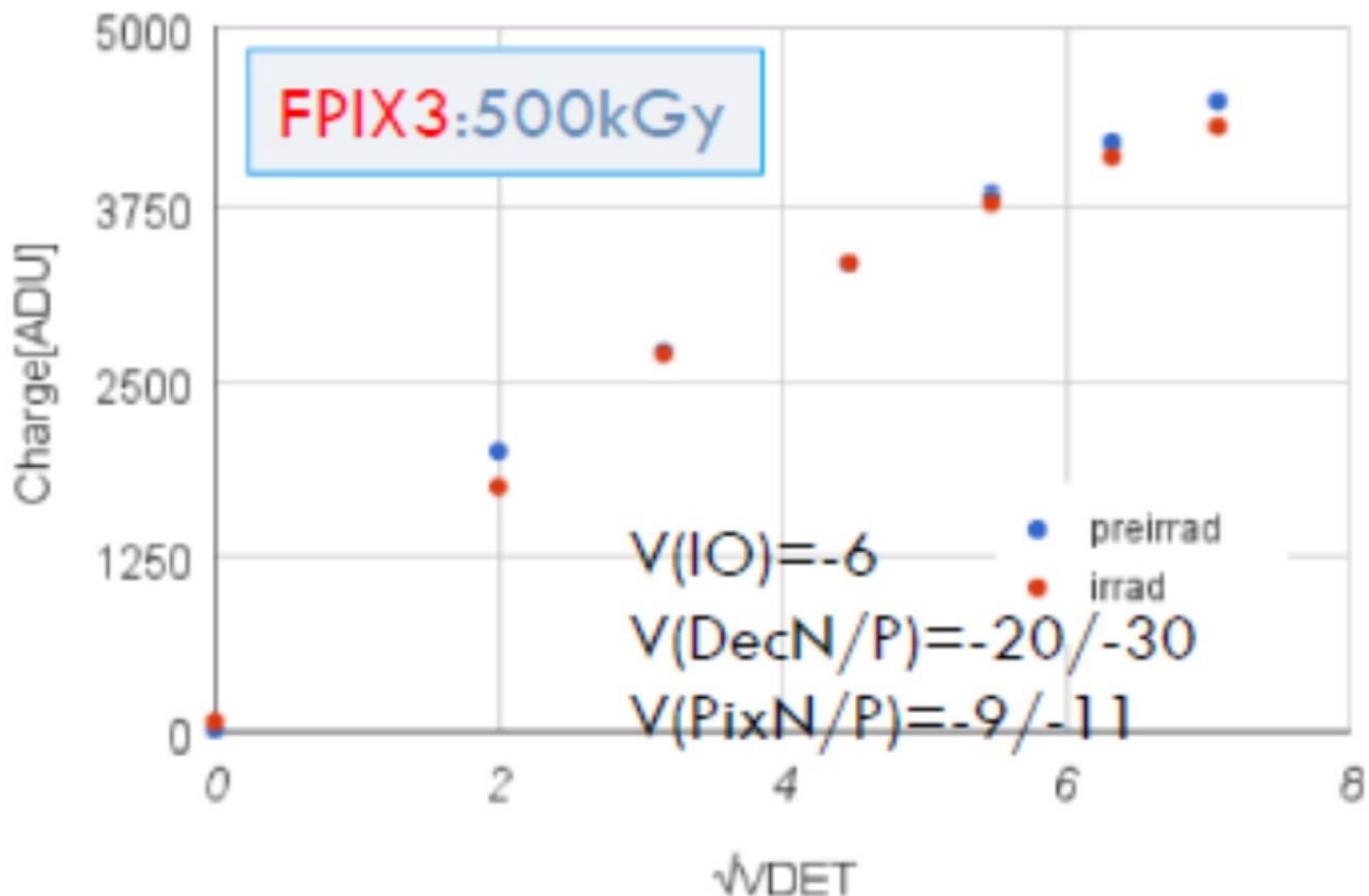
## Recovery of the drain current reduction



By increasing Implantation dose of PLDD region 6 times higher than present value, the degradation is reduced from 80% to 20% at 112 kGy(Si).

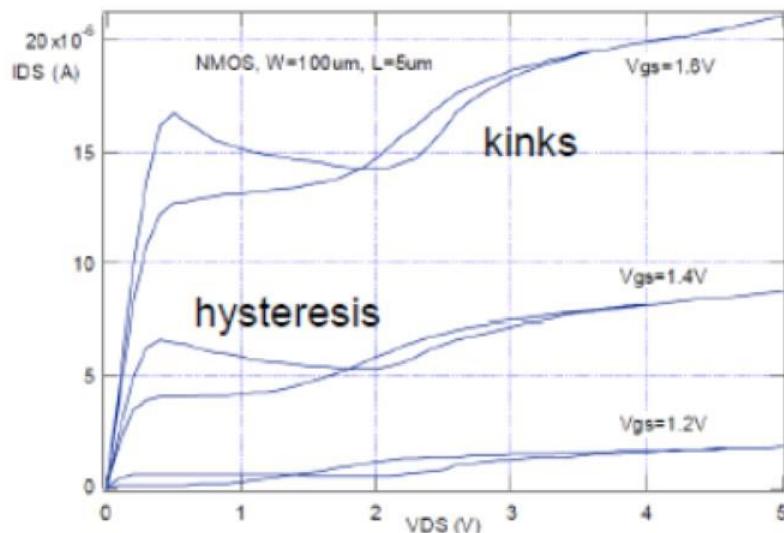
Ref.) I. Kurachi, et al. "Analysis of Effective Gate Length Modulation by X-Ray Irradiation for Fully Depleted SOI p-MOSFETs, IEEE Trans. on Elec. Dev. Vol. 62, Aug. 2015, pp. 2371-2376.

It now looks tolerant  
higher than 50 Mrad radiation

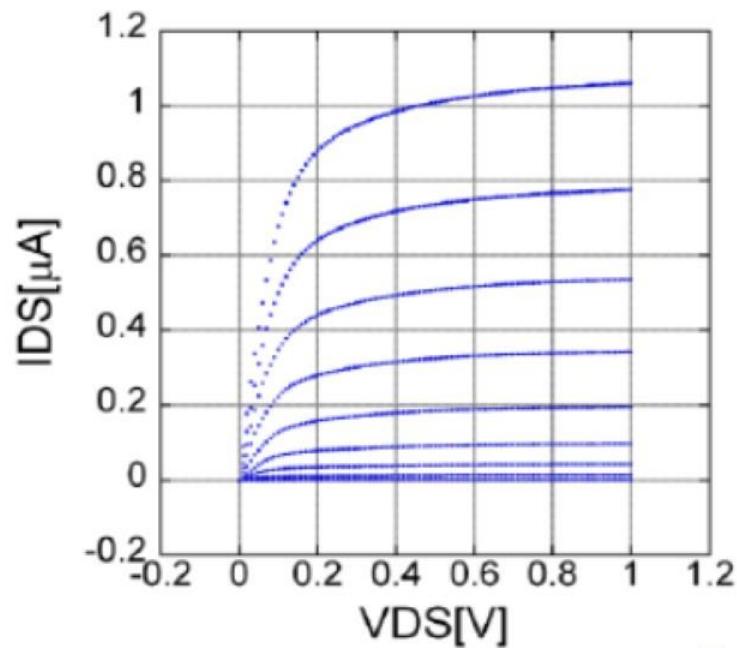


# Operation at Low Temp.

- JAXA, KEK, Tsukuba
- Essential for low temp. sensor circuit for IR, SC sensors.

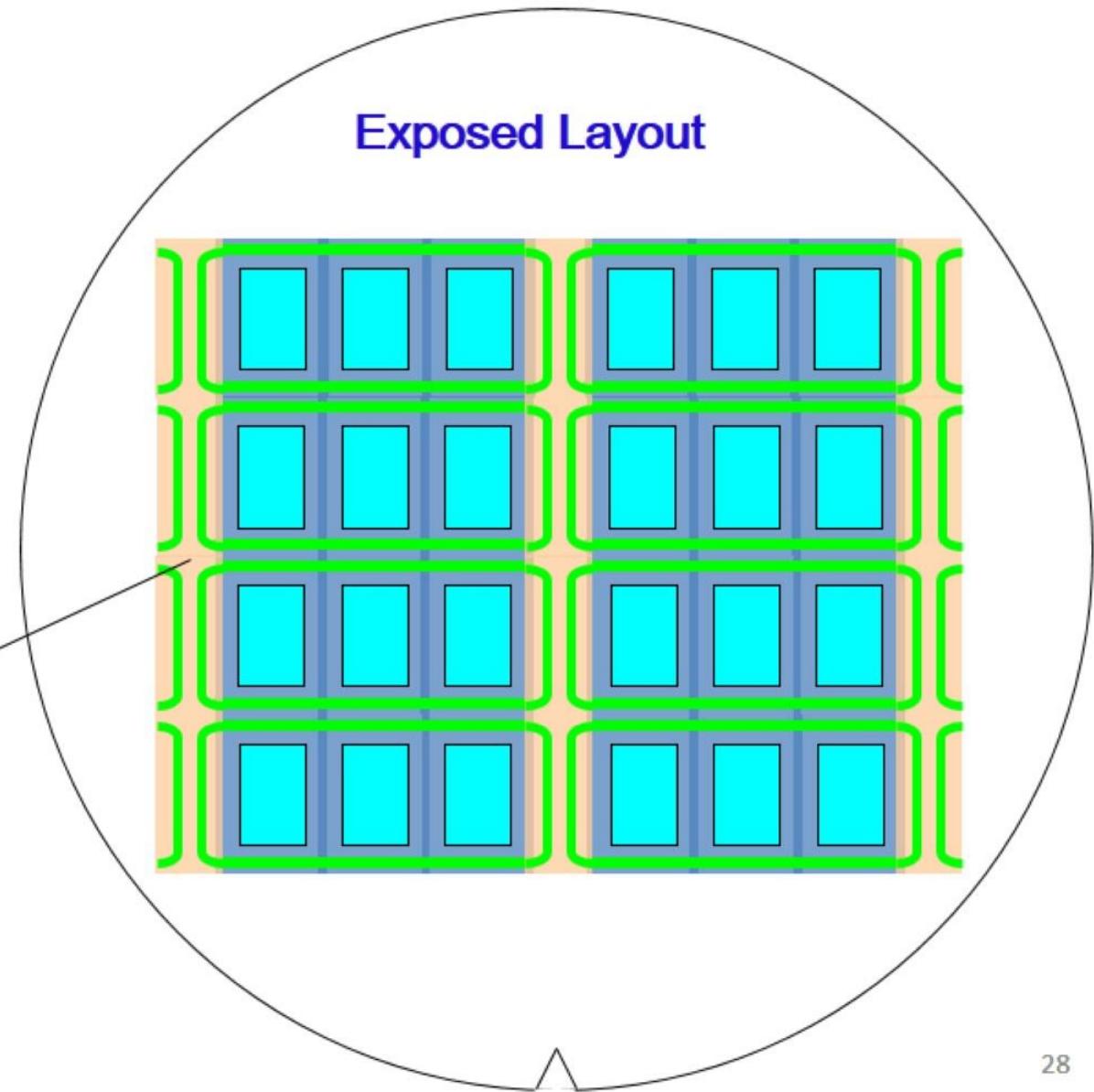
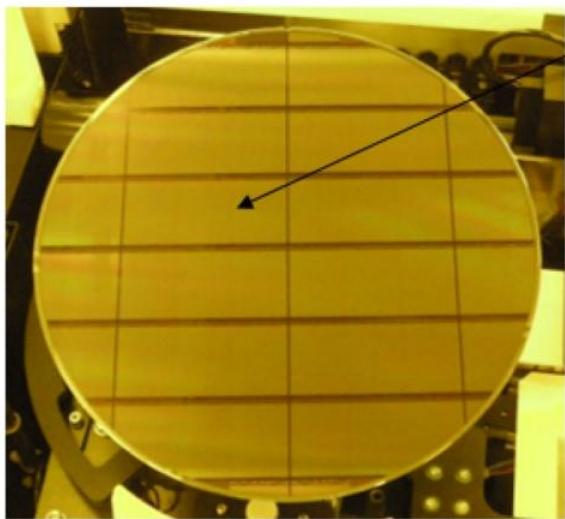
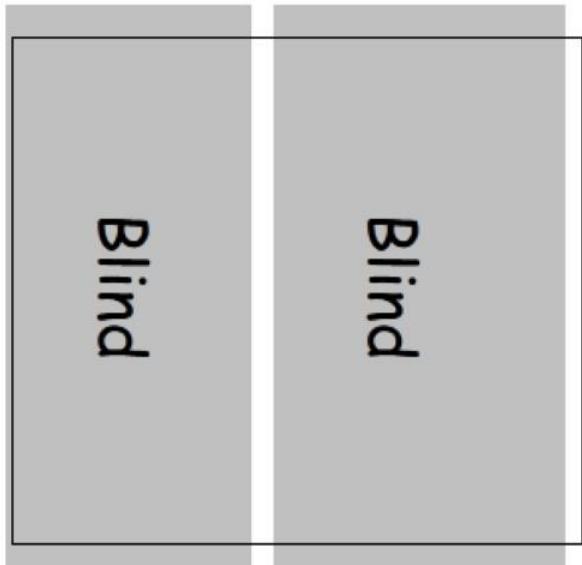


Merken et al. 2004, SPIE 5498, 622



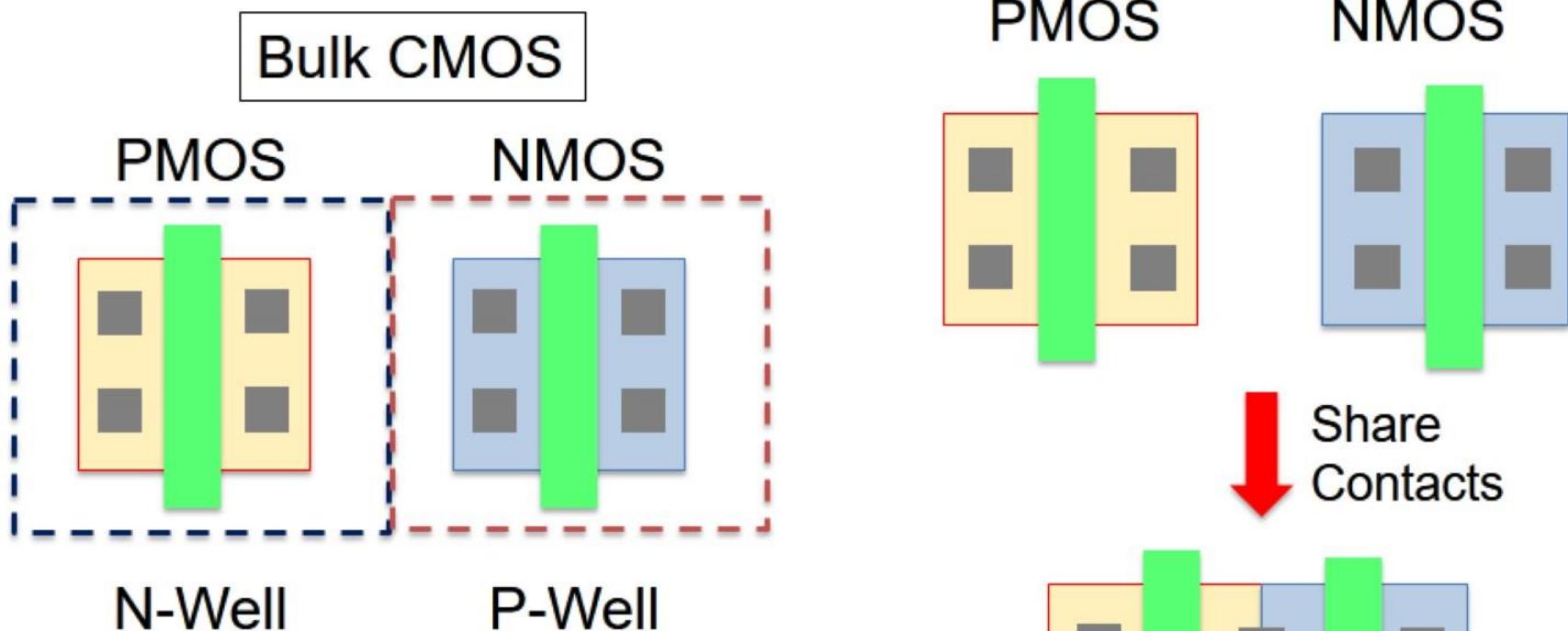
# Stitching Exposure for Large Sensor

## Mask Layout



# Layout Shrink (Active Merge)

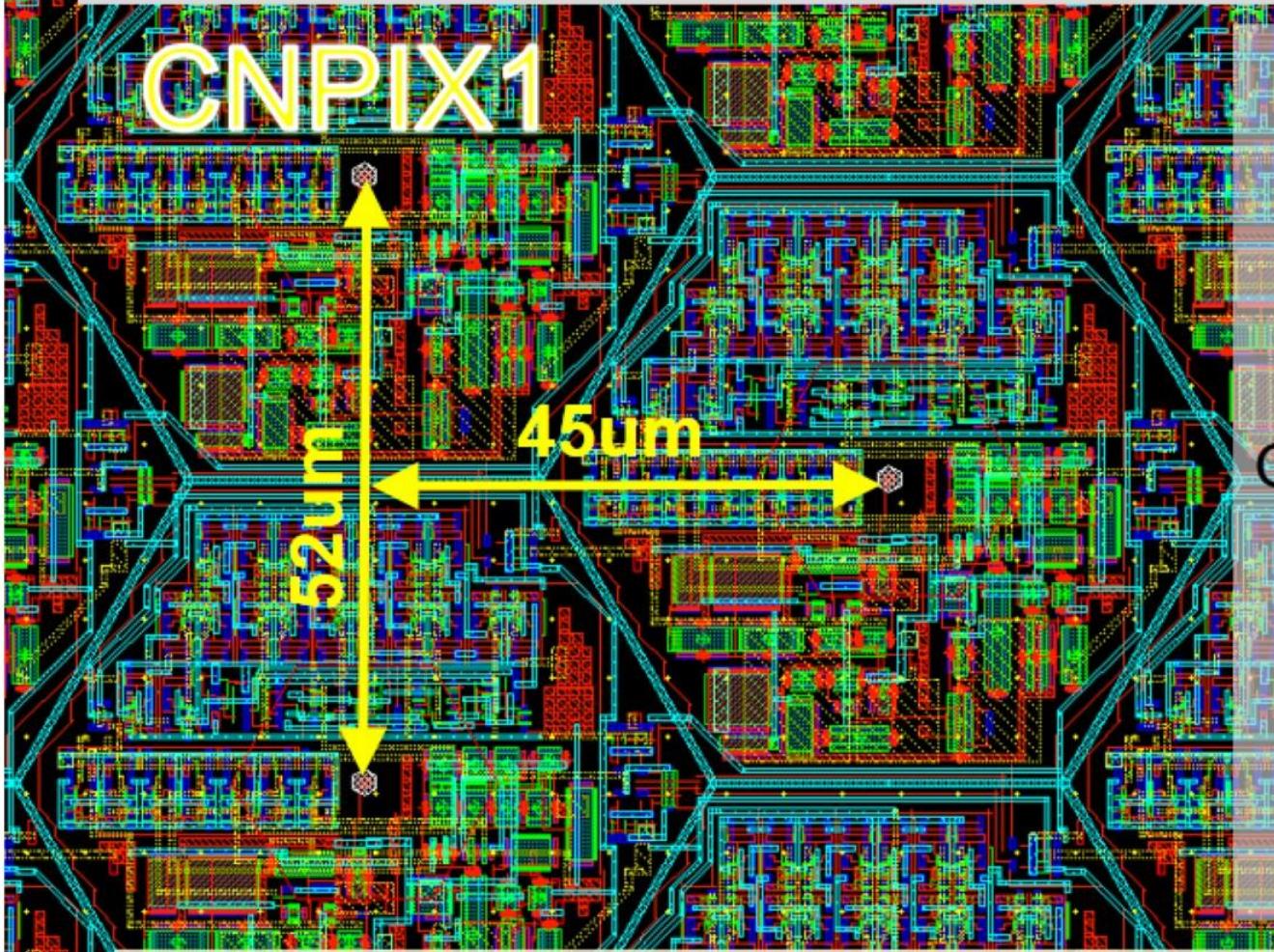
SOI



In the SOI process, it is possible to merge NMOS & PMOS Active region and share contacts.

Salicide Connection

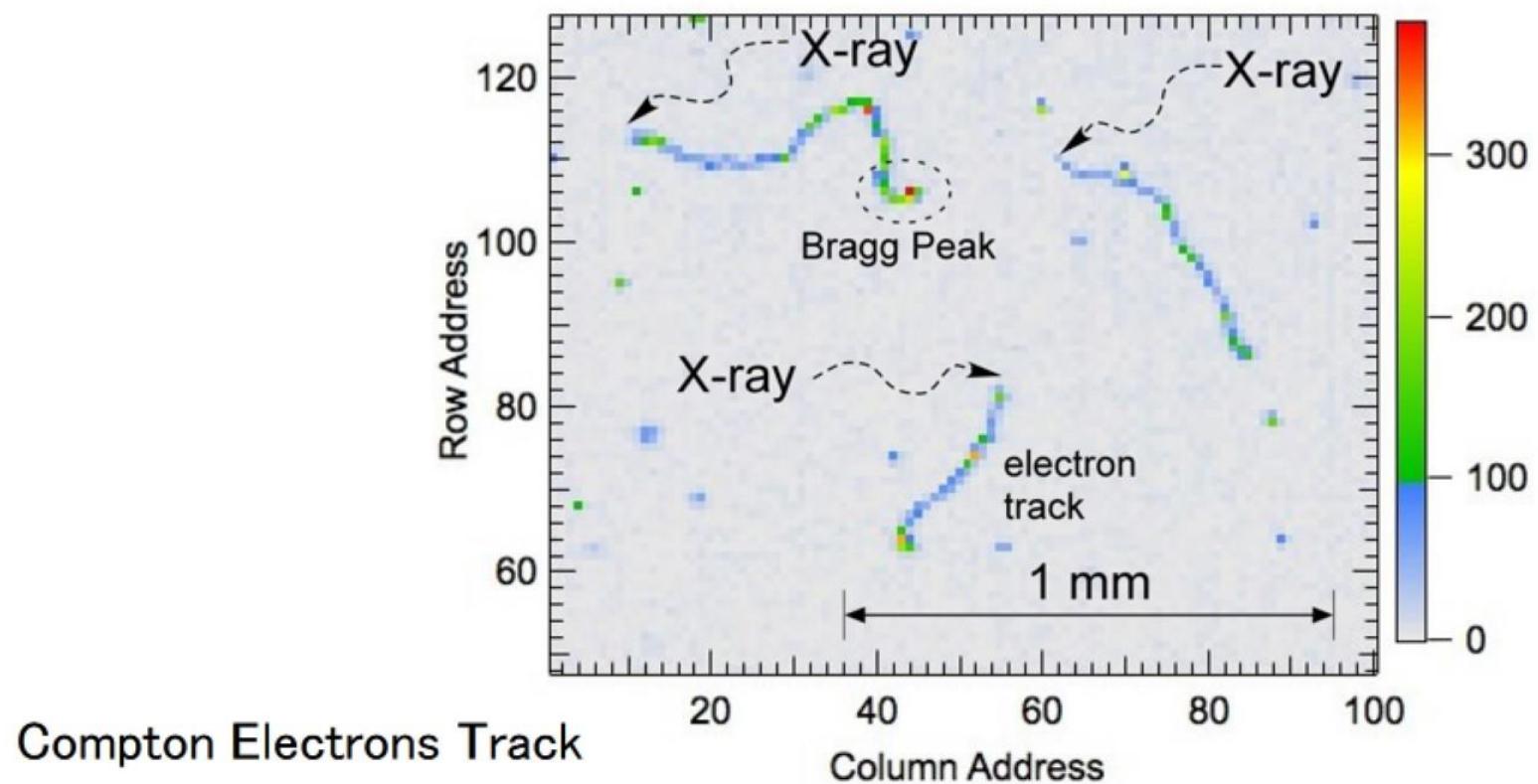
# Hexagonal Counting-type Pixel (submitted in June)



Charge Amp  
+  
Shaper  
+  
Discriminator  
+  
Q Share Handling  
+  
19bit Counter  
+  
7bit register  
(in  $2,340 \mu\text{m}^2$ )

*Smallest Counting-type Pixel of this kind.  
(much smaller than designed in 0.13um process)*

### III. SOI Pixel検出器の紹介



# From Science to Society

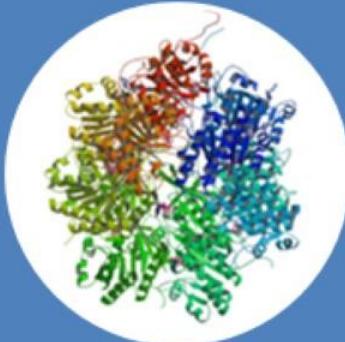


## Fundamental Science (Big Science)

- Advanced Accelerator
- Innovative detector
- HP Computing/Network/
- ASIC development

Only one

➤ 究極の性能  
巨大科学



## Variety of Sciences (medium/small scale)

- Material, Life Science
- Photon and neutron
- Compact accelerator
- Compact detector system

~100

ほどほどの性能・コスト  
研究室の科学



## Industrial , medical ,commercial applications

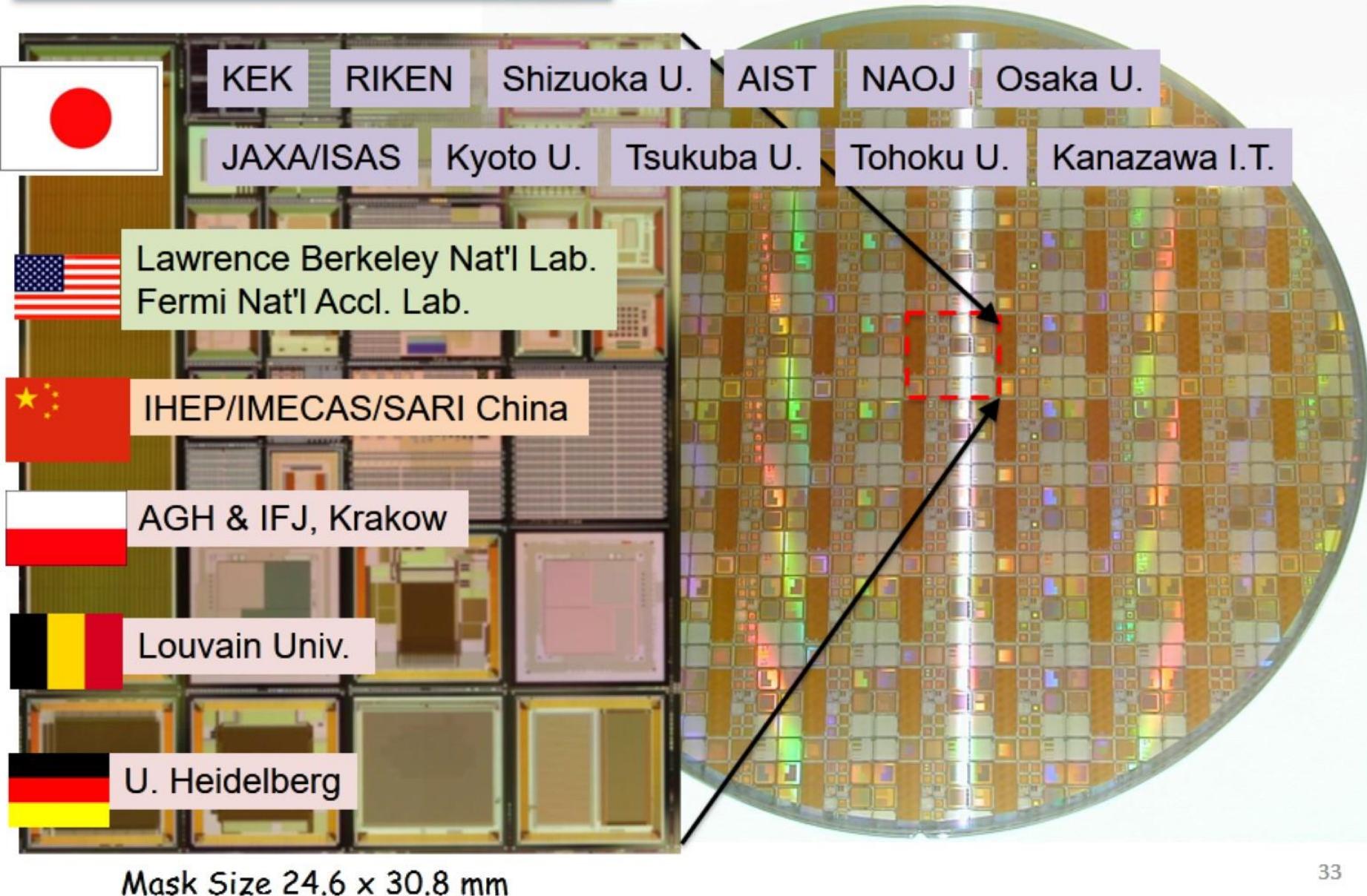
- Reliable, High Yield
- Cost effective
- Mass productive

~100,000 to million

見劣りしない性能  
低成本・信頼性

➤ 民生  
社会応用

# Multi-Project Wafer (MPW) run. (1~2 times/year)

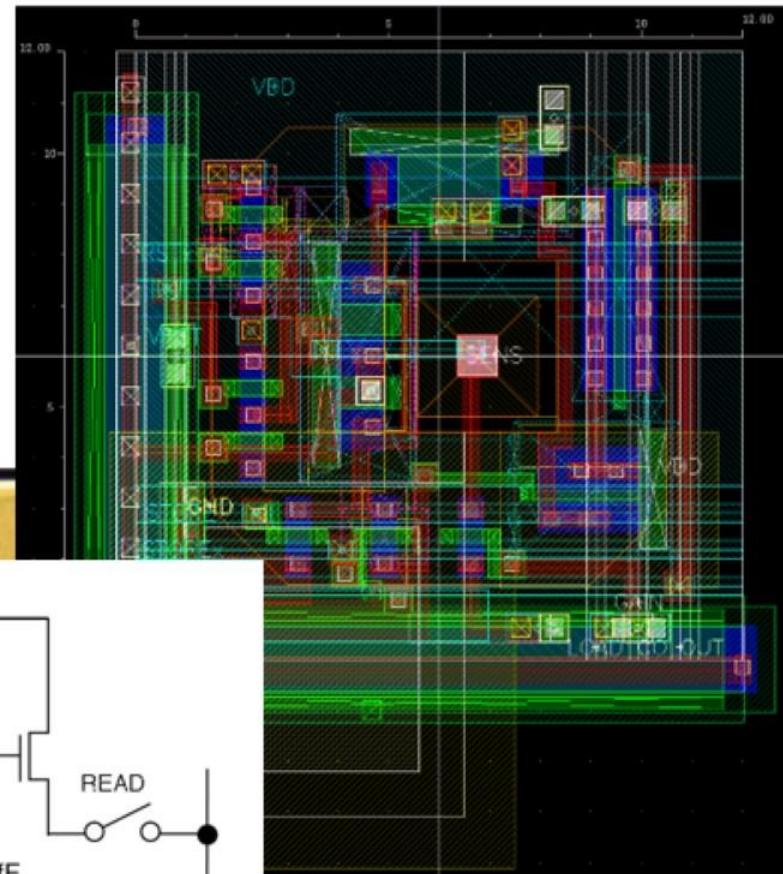
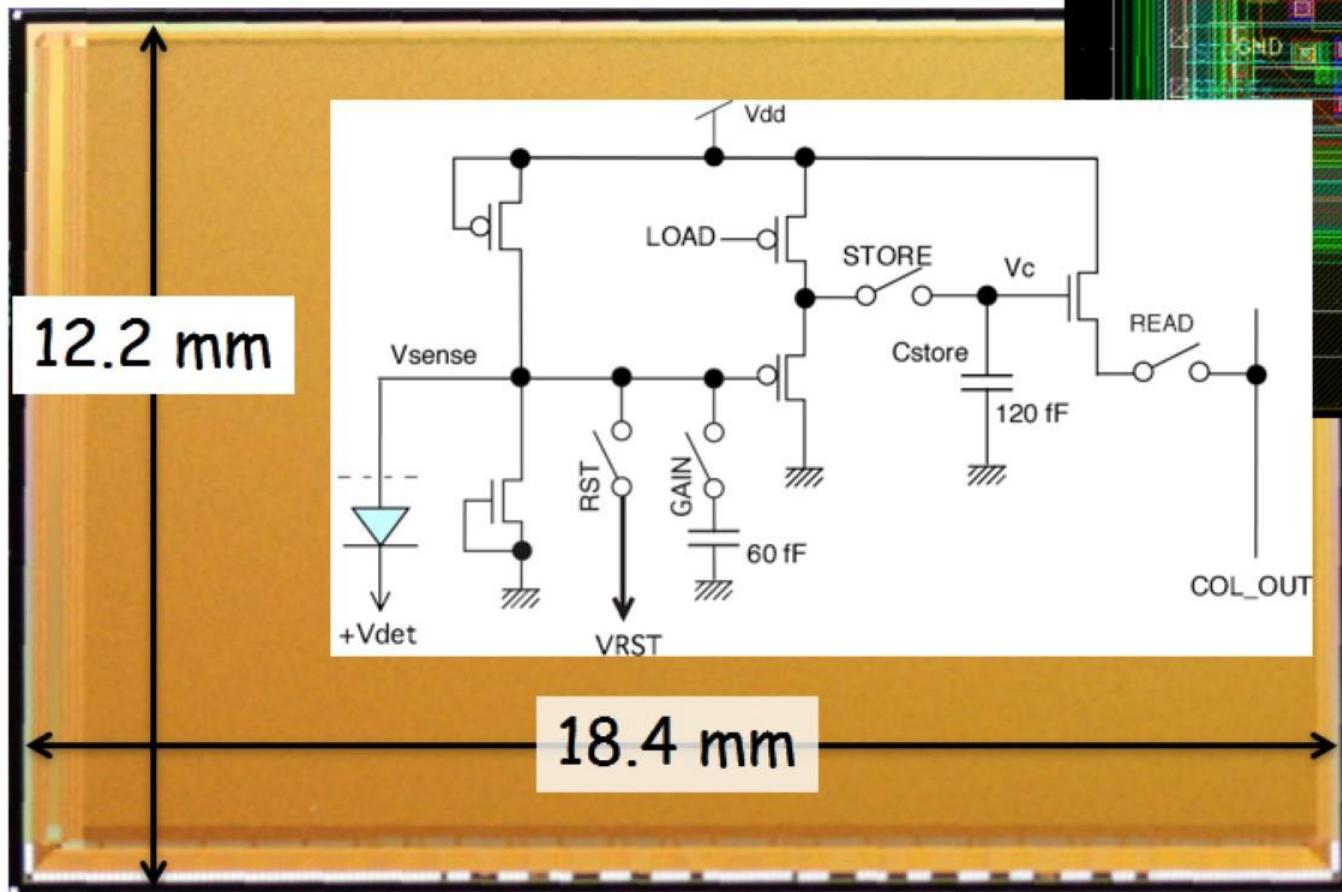


## On-Going SOI Projects

- INTPIX : General Purpose Integration Type → KEK
- SOPHIAS : Large Dynamic Range Large Area for XFEL, SR → Riken
- XRPIX : X-ray Astronomy in Satellite → Kyoto, Shizuoka,,,
- SOFIST : Linear Collider Vertex Detector → KEK, Tsukuba, Osaka, Tohoku,,, (China, Poland)
- CNPIX : General Purpose Counting Type → KEK, China
- STJPIX : Superconducting Tunnel Junction on SOI → Tsukuba Univ.
- MALPIX : TOF Imaging Mass Spectrometer → KEK, Osaka Univ.
- ...

# Integration Type Pixel (INTPIX)

Pixel Size :  $12 \times 12 \mu\text{m}^2$   
896x1408 (~1.3 M) pixels,  
11 Analog out port, Column CDS.



INTPIX5

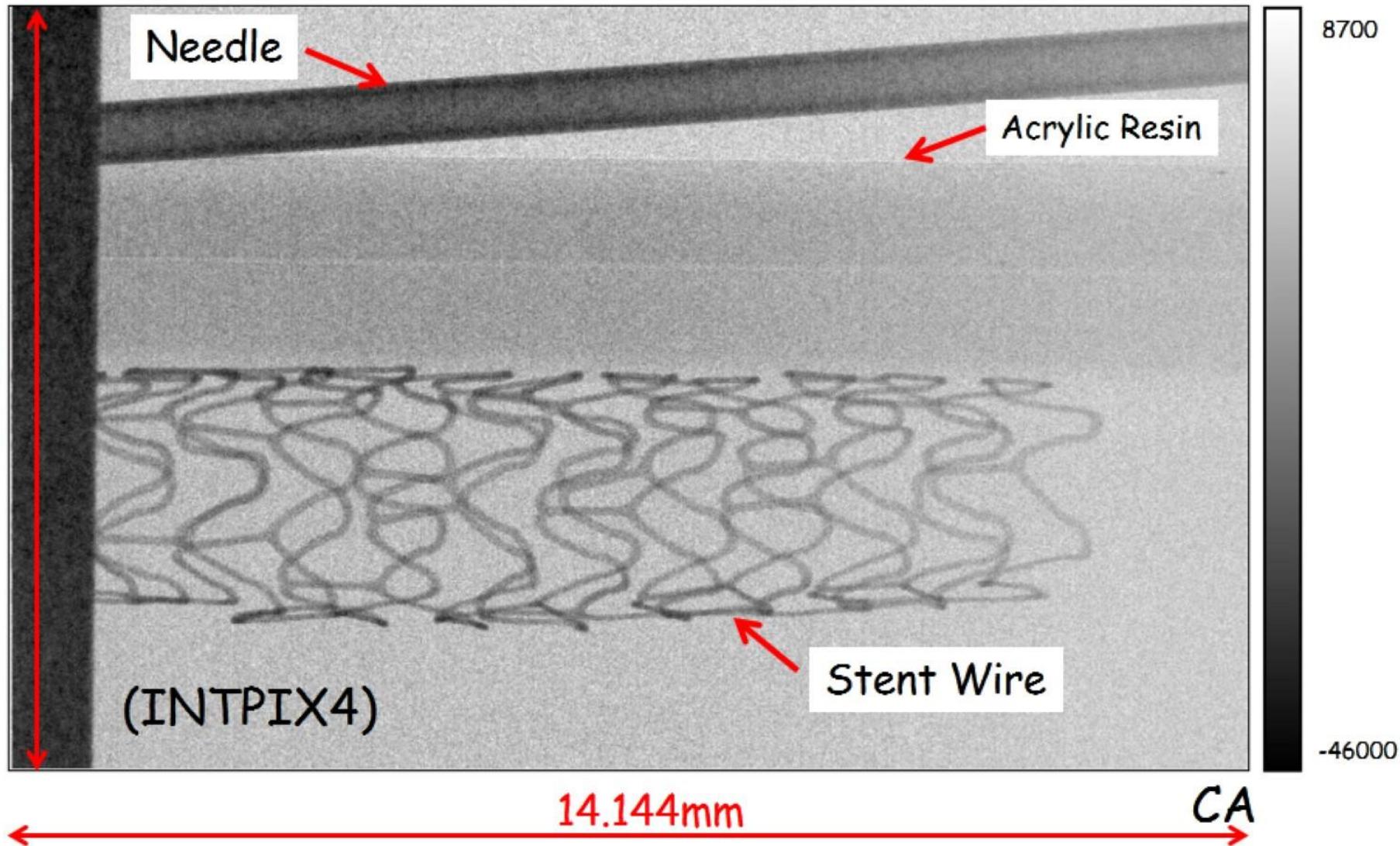
## X-ray Image with the INTPIX

PF-AR NE7A 33.3keV  
Acrylic resin 40mm  
200us x 250 frames

Arb. unit

RA

8.704mm

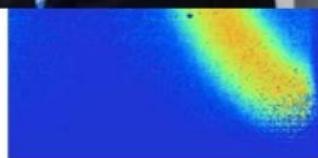


佐々木、三井(金沢大)

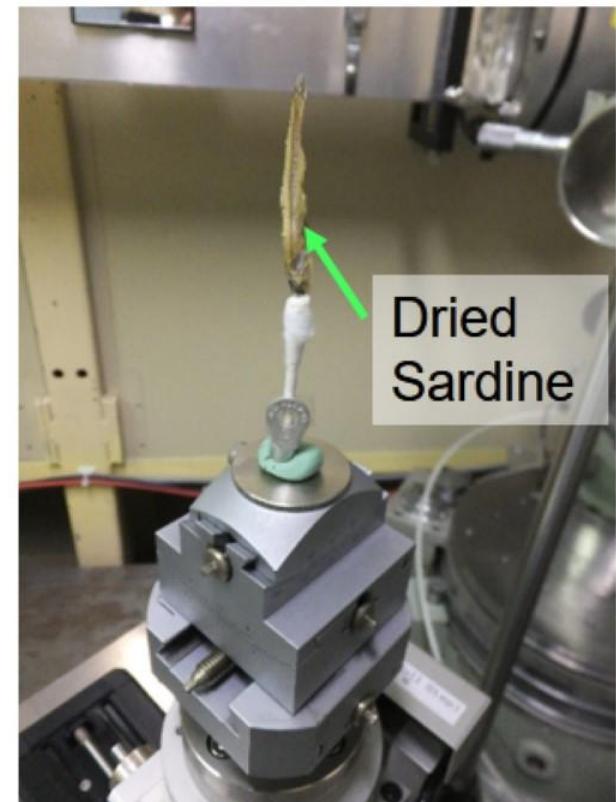
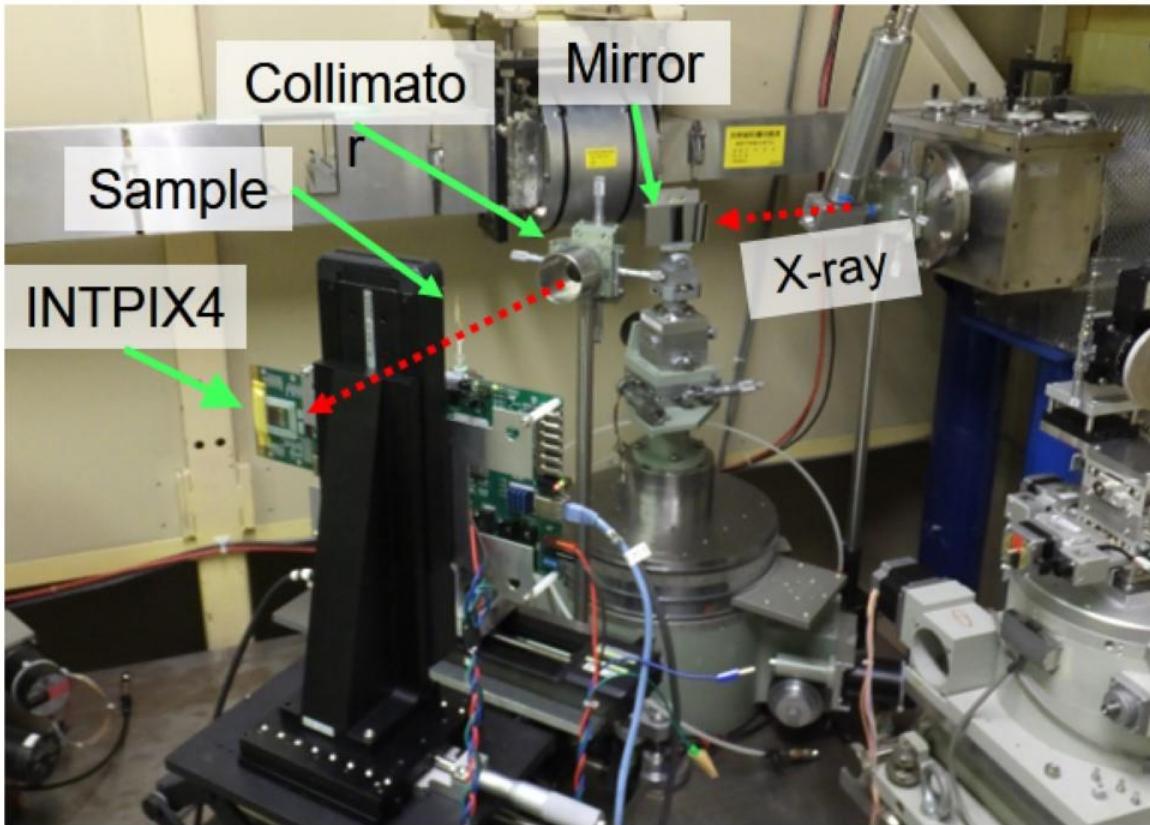
# SOIピクセルによる X線金属疲労測定



回折環の測定  
二次元計測

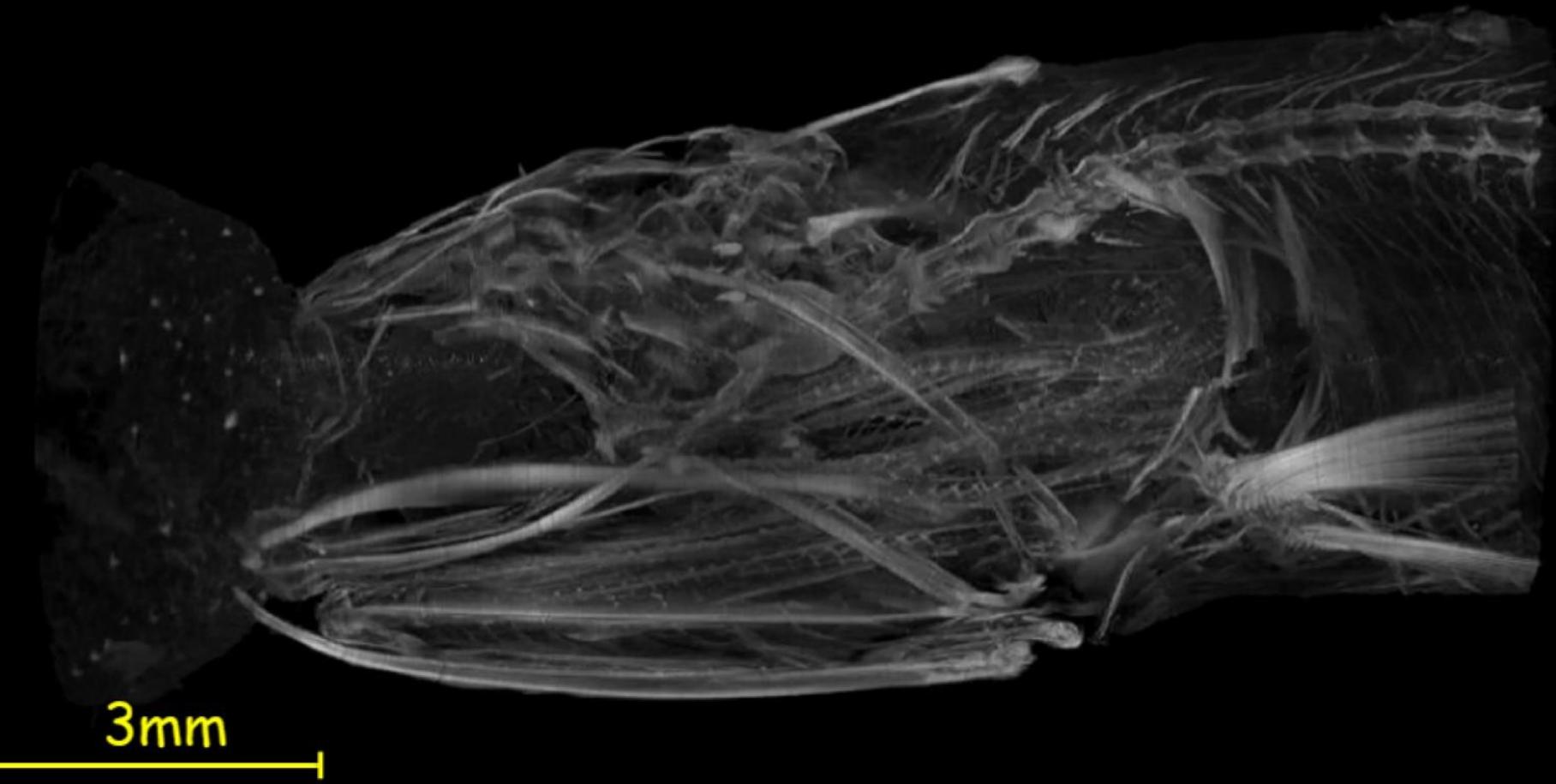


# 3D Tomography with Synchrotron X-ray



- Sensor: INTPIX4 FZn, Backside Illumination
- HV: 200V, Integration Time: 1ms, ScanTime: 320ns/pix, 1000frame/event
- KEK PF, X-ray Energy: 9.5keV
- Took images for  $0^{\circ}$ ~ $180^{\circ}$  at every 1 degree.

## INTPIX4: Computed Tomography with Syncrotron X-ray

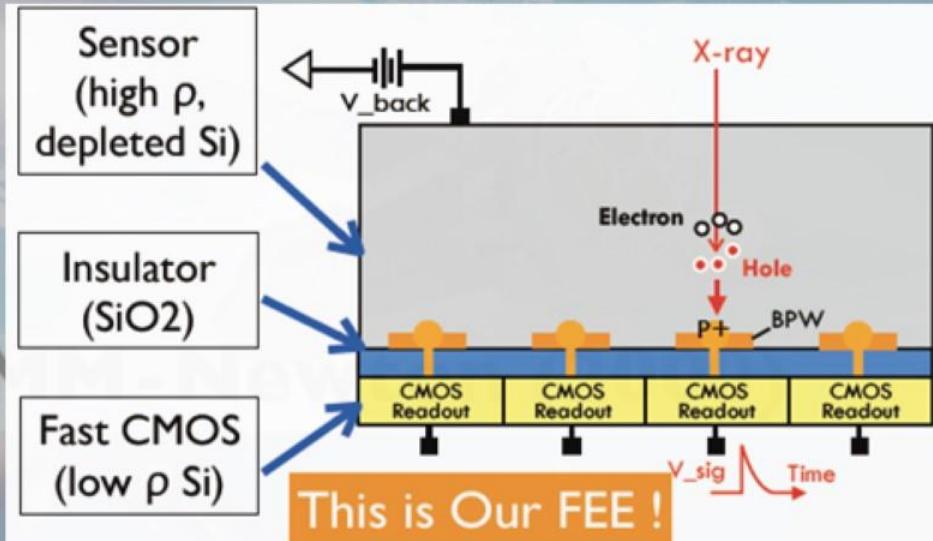


(by R. Nishimura, K. Hirano (KEK)

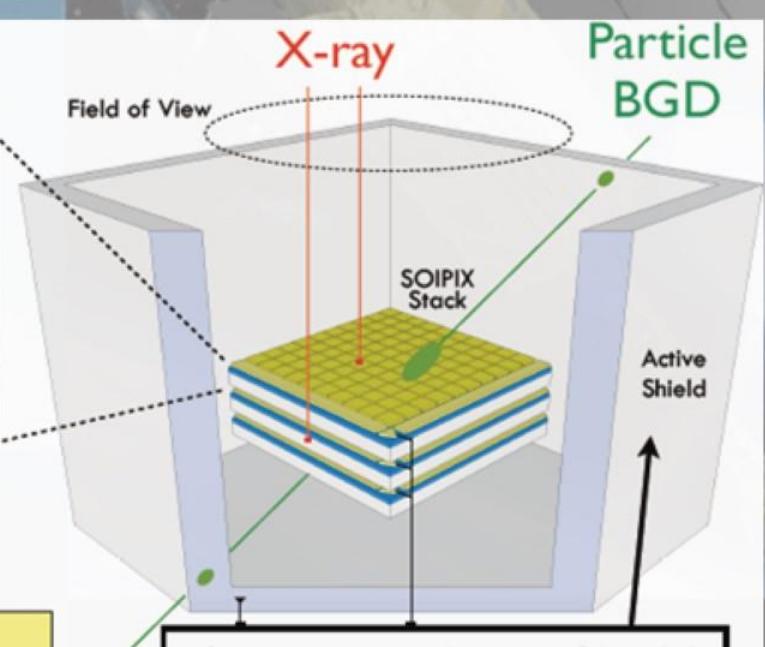
## XRPIX (SOI Pixel sensor for X-ray Astronomy)

Timing resolution of CCD is too poor to make anti-coincidence.

**Chandra (1999)**



Each pixel has its own trigger and analogue readout CMOS circuit.

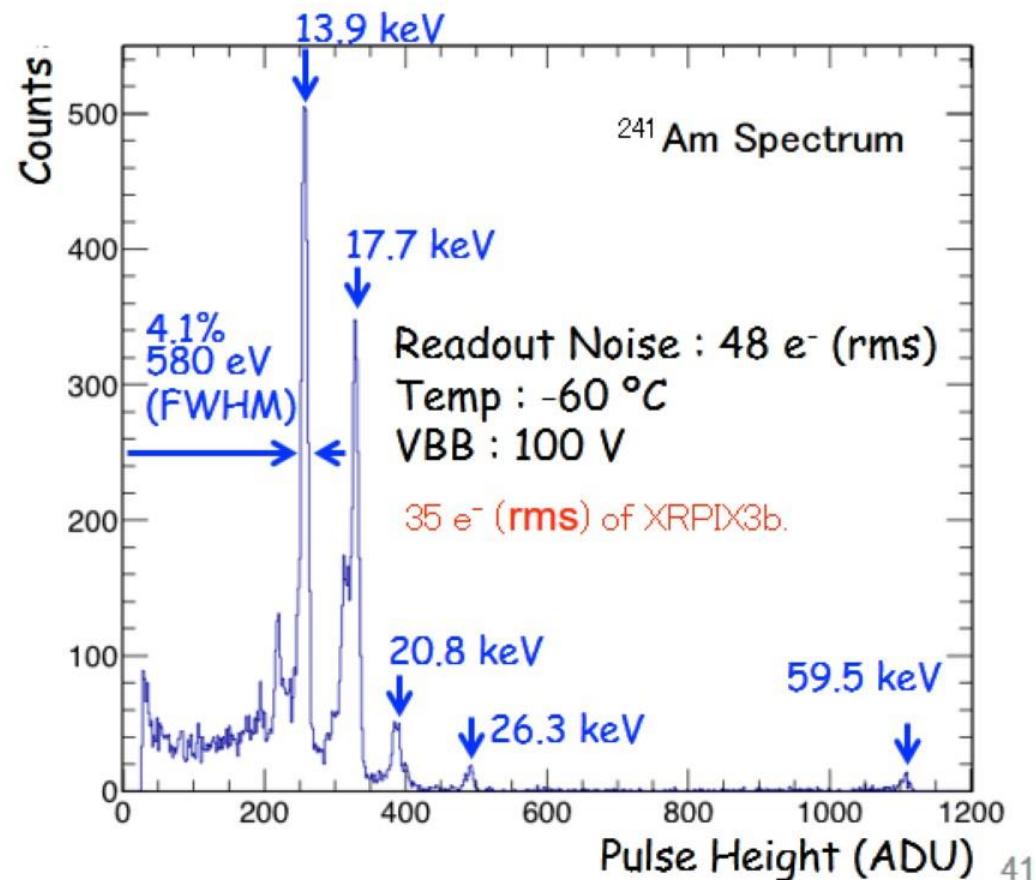


FORCE (Focusing On Relativistic universe and Cosmic Evolution)衛星へ

# XRPIX5: Event Driven X-ray Astronomy Detector



- Chip size : 24.6 mm x 15.3 mm
- Pixel size : 36  $\mu\text{m}$  sq.
- # of pixel : 608 x 384 (= ~233k)
- Thickness of sensor layer : 310  $\mu\text{m}$  (CZ wafer)  
500  $\mu\text{m}$  (FZ wafer)

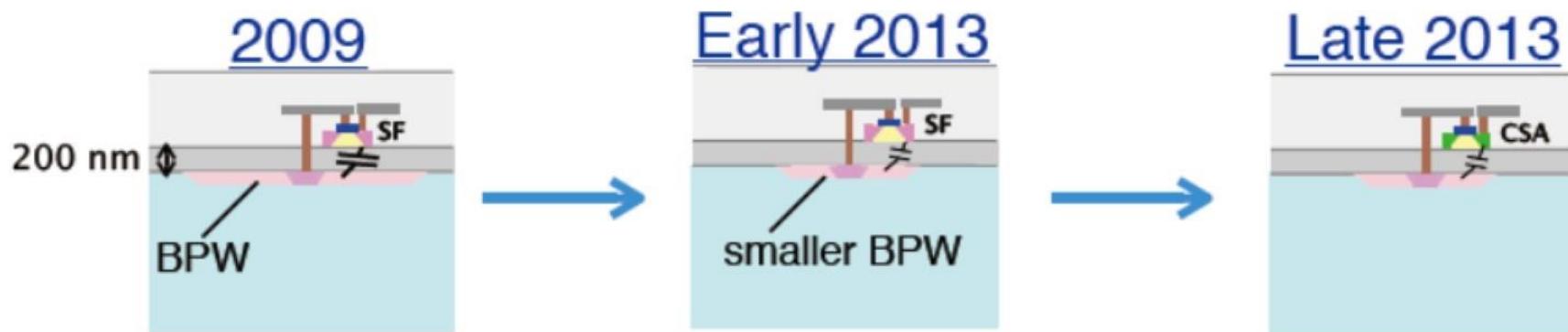


# Improvement of Spectral Performance in Frame Mode

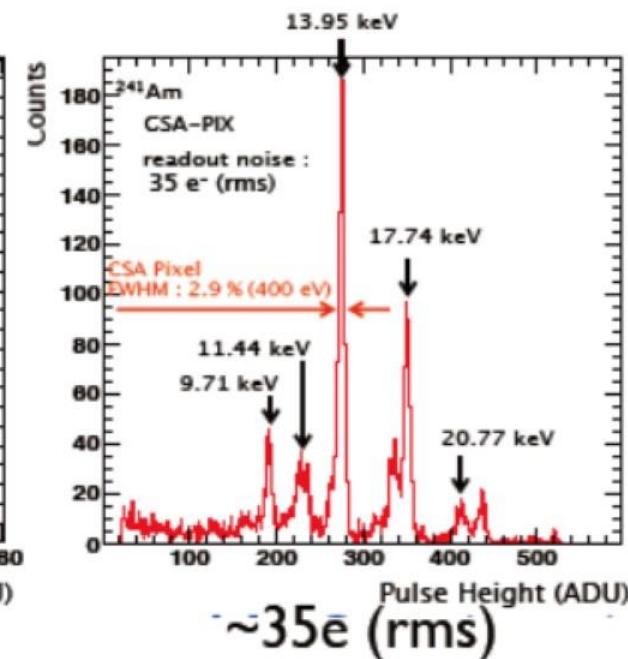
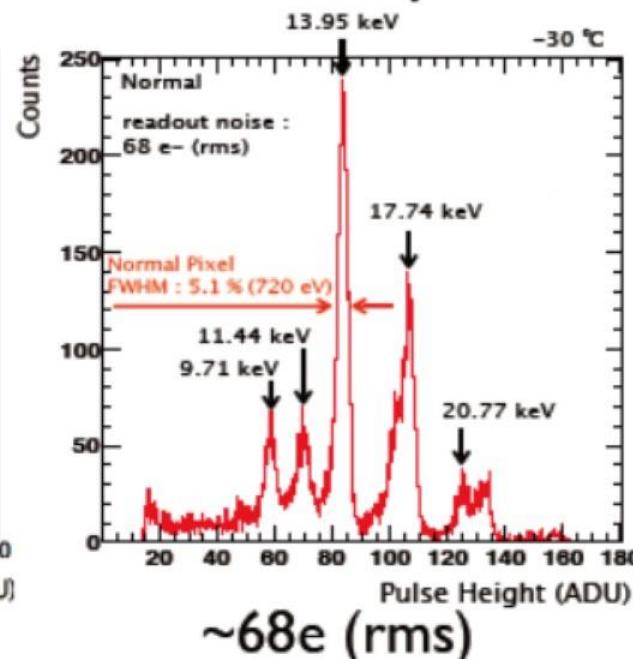
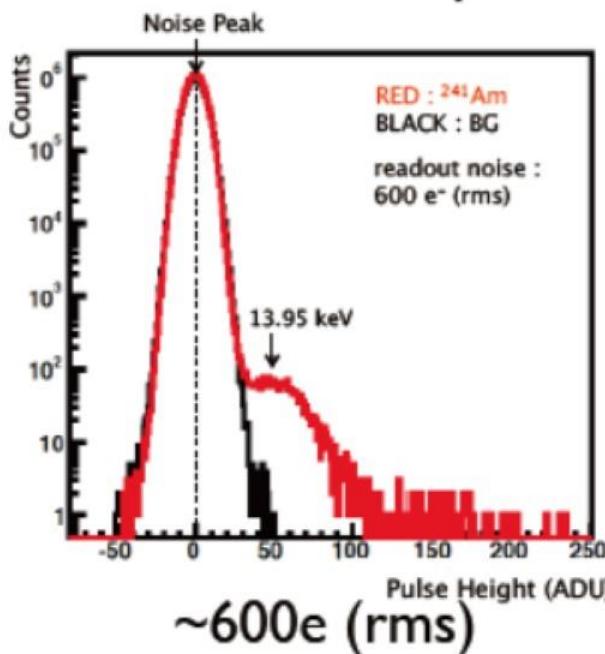
15

increase the node-gain by applying smaller BPW (parasitic Capacitance).

Introduction of in-pixel charge-sensitive amplifier



Spectra of Am-241 X-rays in Frame mode



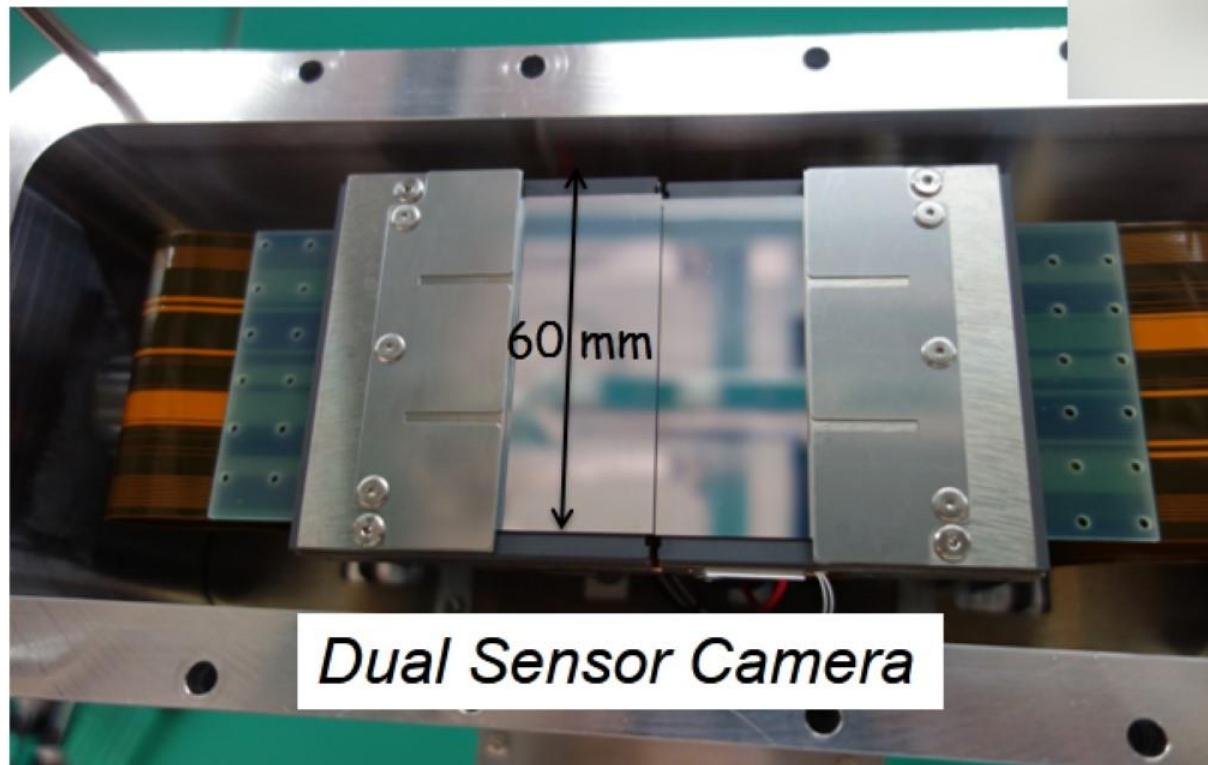
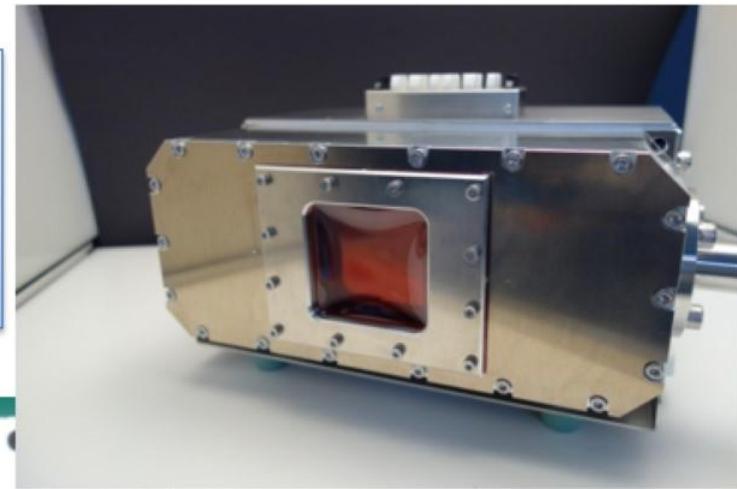
# SOI Photon-Imaging Array Sensor (SOPHIAS) for X-ray Free Electron Laser (XFEL) SACLA

SPRING-8

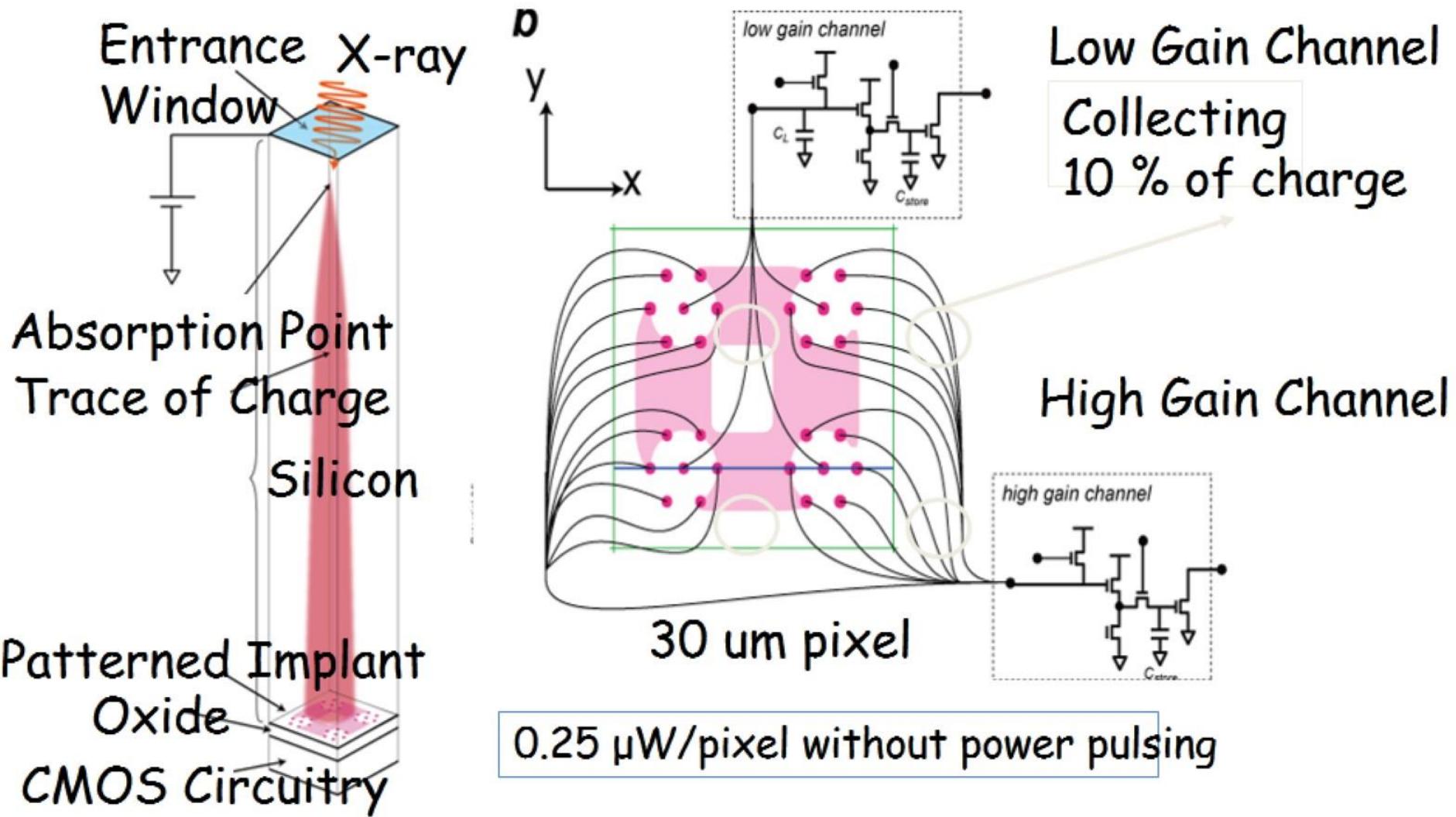


Utilization of SOPHIAS has been started for various experiments in SACLA@RIKEN.

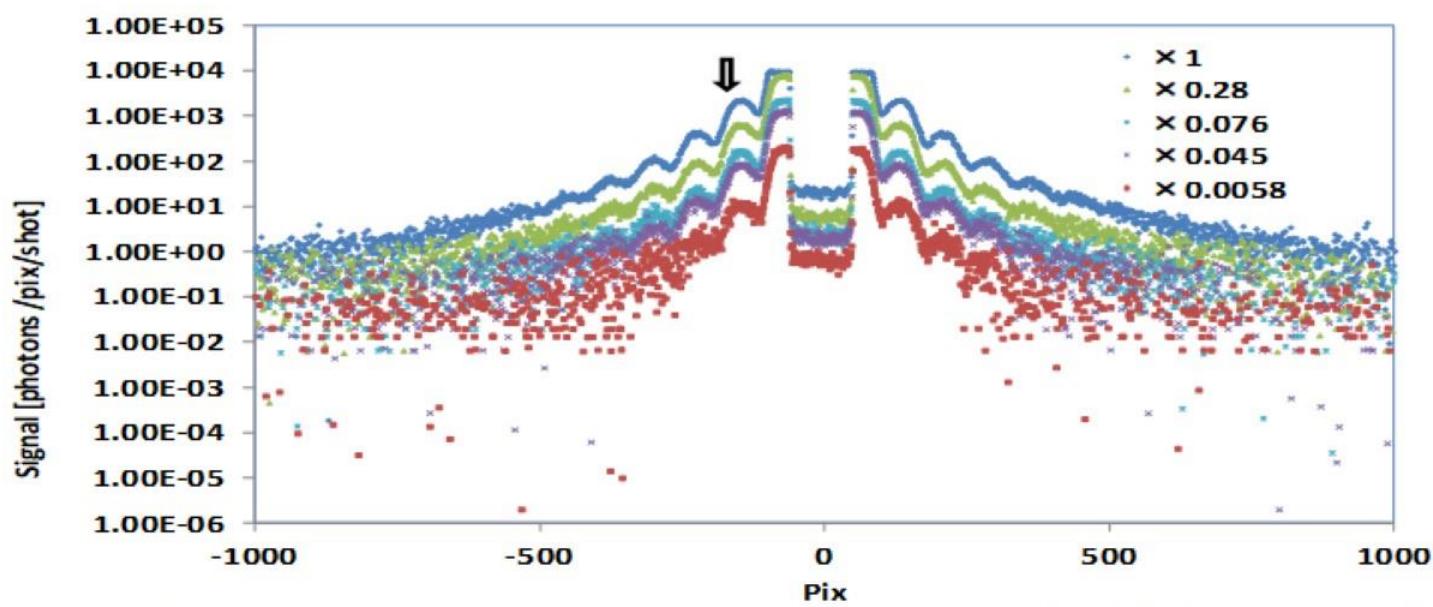
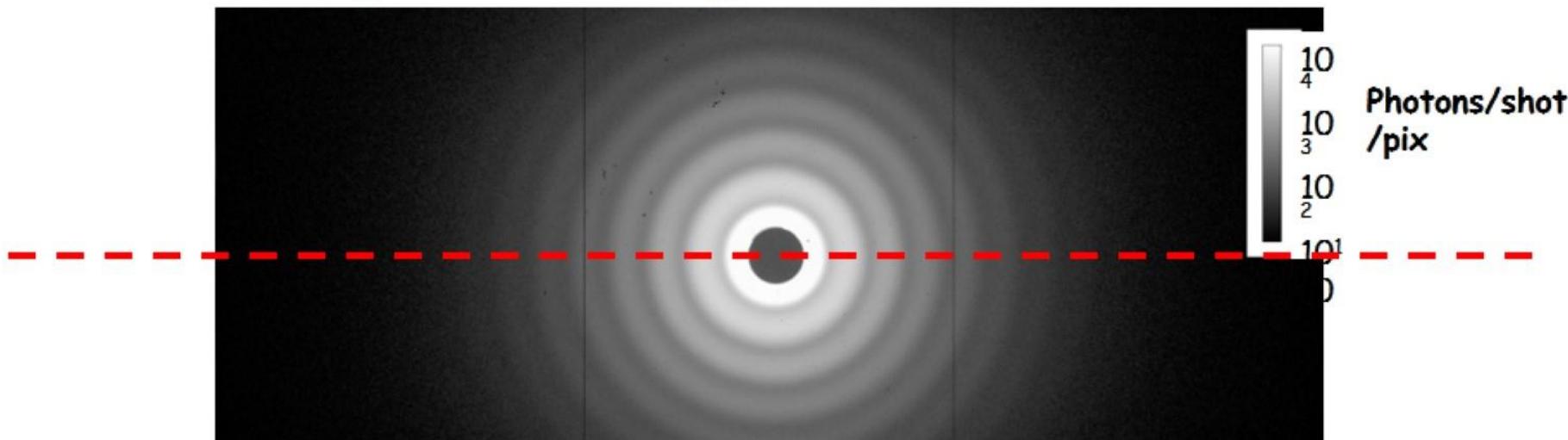
- Dynamics of Atomic Structure
- Direct Observation of Chemical Reactions
- etc.



# Implementation: Charge Collection



$\text{SiO}_2$  nano particle,  $D=17\text{nm}$   $E=8\text{keV}$   
Small angle scattering

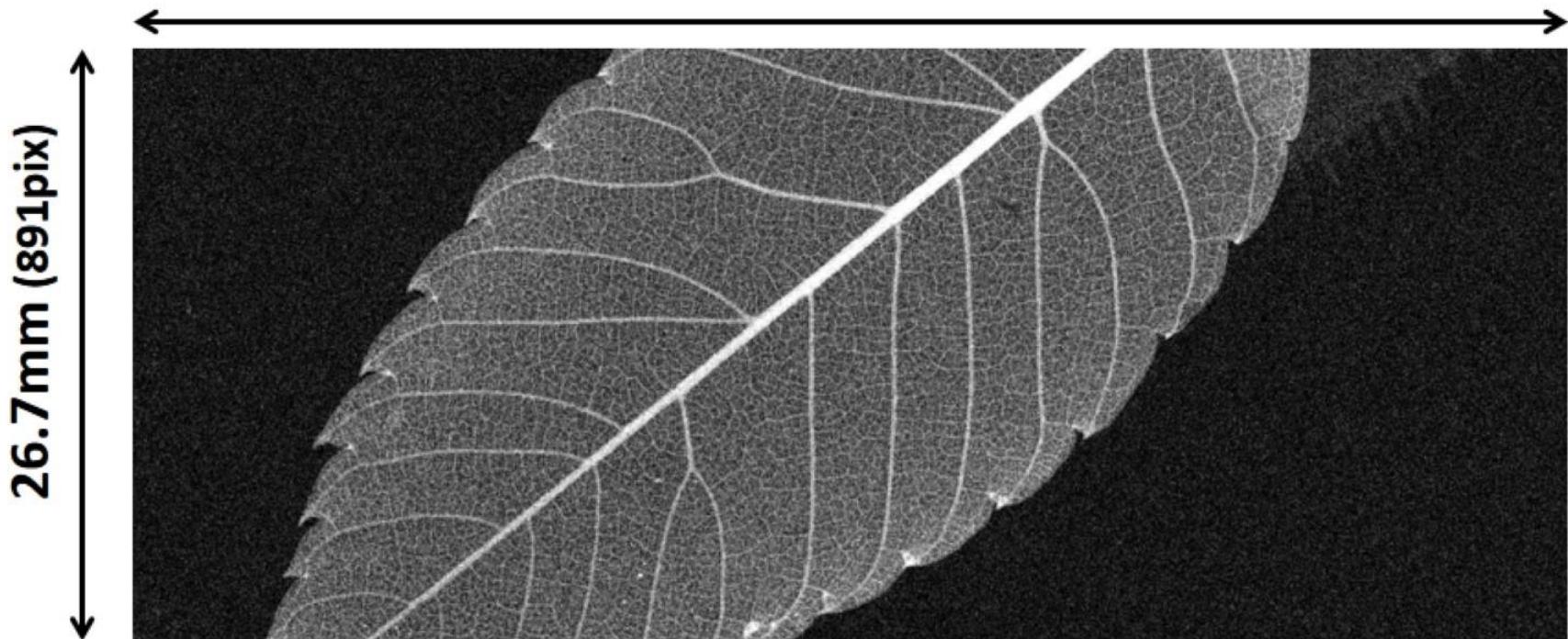


Beam Intensity to sample  $3 \times 10^{12} \text{photons/s}$

Beautiful  
High gain Image!

Pix size : 30um × 30um

**64.8mm (2160 pix)**



**22kV 200uA Target Cu K $\alpha$  8keV  
1000 shot averaged**

**0.5 photon/pix/shot**

**1.9M pixels !!**

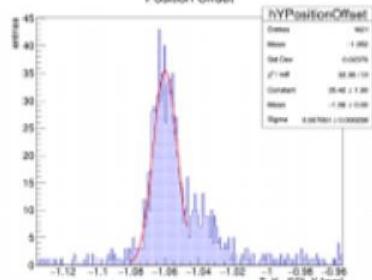
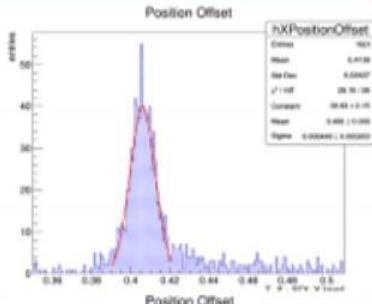
# Pixel for future Collider

- SOI pixel is now one of the most promising LC vertex detectors

## CLICdp by AGH in SOIpix collaboration

Results from June test beam – standalone analysis

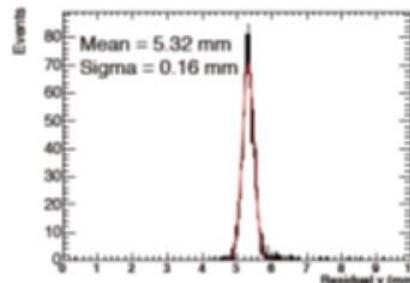
- Very first results show **spacial resolution** on the level of **6-7  $\mu\text{m}$**  (pixel pitch 30  $\mu\text{m}$ )
- Significant **improvement is expected**
  - No bad pixel rejection
  - No rotation correction
  - Preliminary results obtained for the whole matrix (different pixel architectures doesn't taken into account – **differences in gains not included**)



## For ILC by KEK

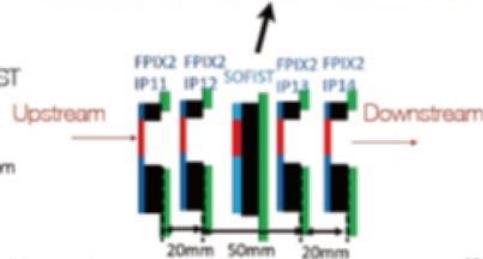
### SOFIST ver.1 Beam Test

Residual between expected and actual hit position on SOFIST ver.1.



Multiple scattering at the slave DAQ board, a socket, and a ceramic package for SOFIST are causes of coarse spatial resolution.

However we successfully constructed the entire system for charged particle tracking.



# Comparison to previous studies

"Physical limitations to the spatial resolution of solid-state detectors", M. Boront et al., IEEE TNS 62-1, p381 (2015)

"a simple formula  $\sigma \sim p/(S/N)$  saturates due to  $\delta$  electrons at higher S/N"

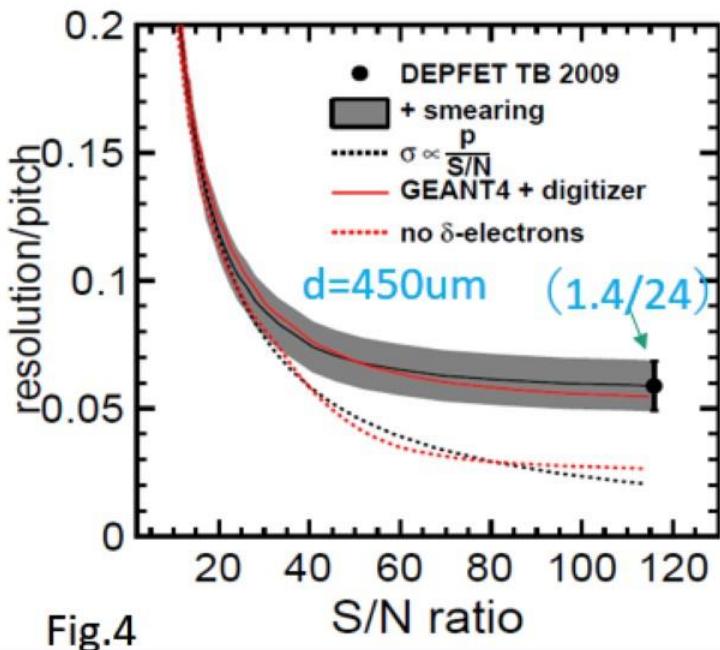
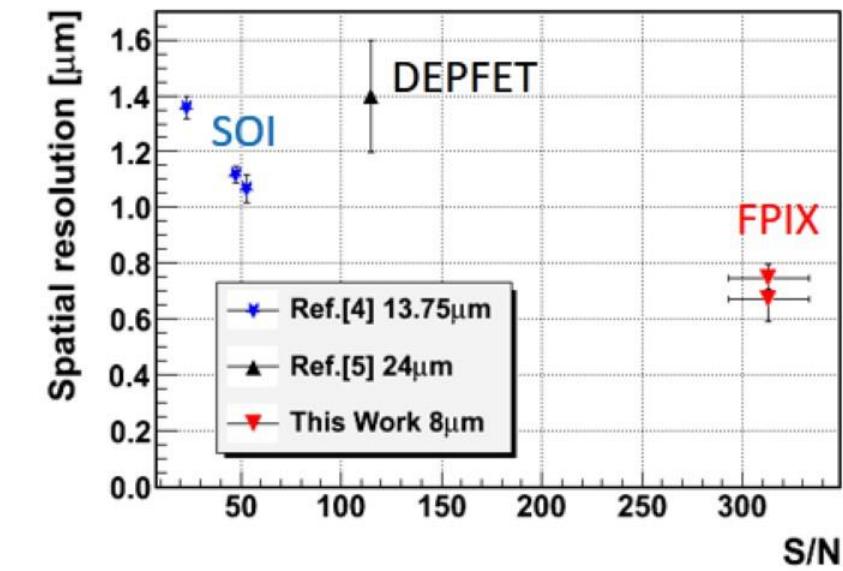


Fig.4

Other device with  $\sim 1\mu\text{m}$  resolution  
13.75 $\mu\text{m}$  pixel (SOI)  $\Rightarrow 1.07 \pm 0.05 \mu\text{m}$   
M.Battaglia et al., NIMA676,50(2012)

Using a combination of Monte Carlo simulation and test beam data we establish that energetic electrons forming secondary tracks known as  $\delta$ -electrons limit the resolution to the level of approximately  $1 \mu\text{m}$ , checking the improvement of the resolution with increasing S/N ratio predicted by [2]. It seems impossible, therefore, to produce position-sensitive devices based on interpolation of the signal in adjacent pixels or strips with a resolution significantly below  $1 \mu\text{m}$ .



FPIX2 achieved a sub-micron spatial resolution

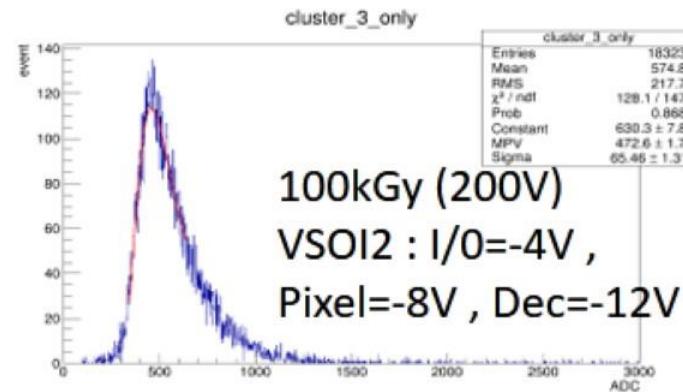
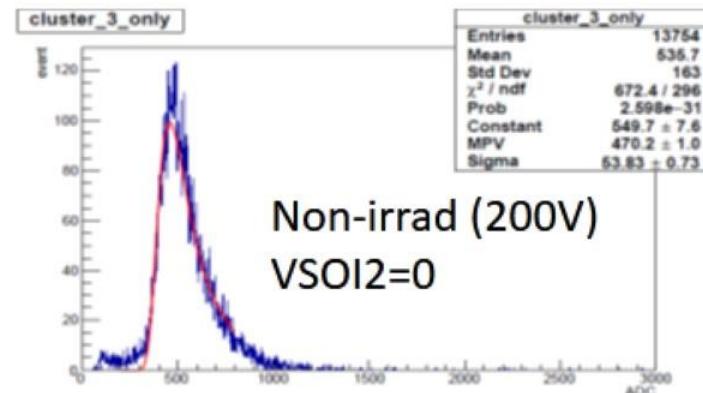
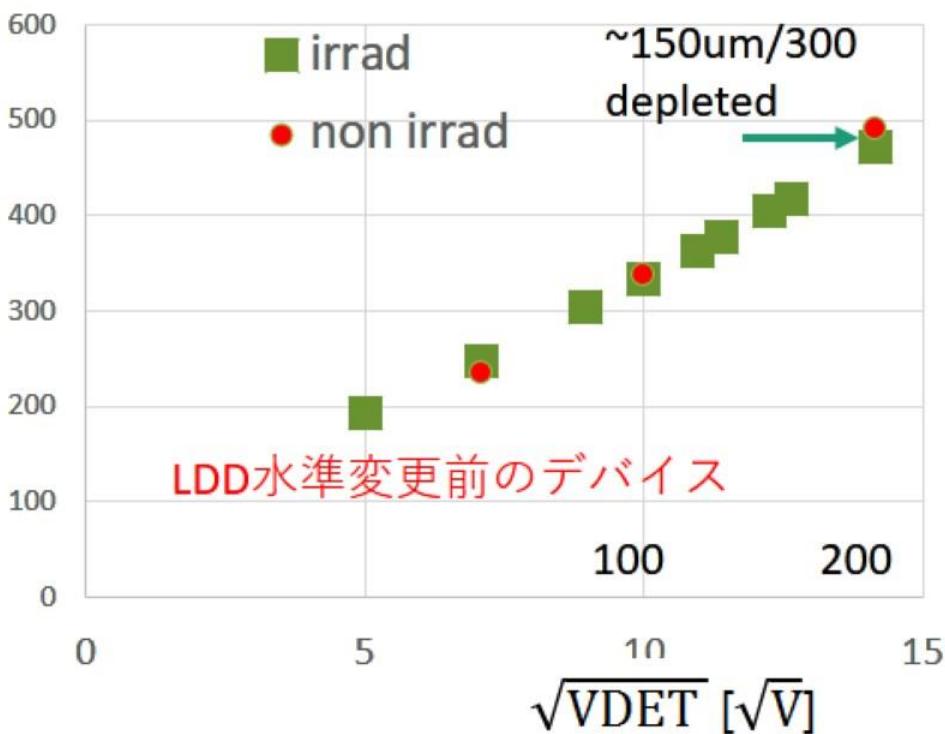
# FPIX2:DSOI 100kGy



for ILC, Belle II

5x5 cluster charge about the maximum charge pixel in an event

## 5x5 cluster charge [ADC]



Innovative double-SOI allows operation of SOI devices to 100kGy  
Recent study extended to 1MGy

## IV. まとめ

- ・測定器開発室プロジェクトとしてSOI Pixel検出器開発をスタートし、現在新学術領域研究を中心に様々な検出器を開発している。
- ・SOI検出器に特有な様々な課題を克服することで、世界で初めて実用的なSOI放射線イメージセンサーをKEKで開発した。
- ・SOI Pixel プロセスはSiセンサーと集積回路を一体化した半導体プロセスで、飛躍的な性能向上と多くの応用が考えられる。
- ・検出器開発には多くの時間と費用がかかることから、今後もコミュニティからの大きなサポートが必要。